RISC-V opportunity, innovation, and collaboration igniting HPC

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ISC, June 2025

RISC-V is the industry standard ISA that **expands opportunity**

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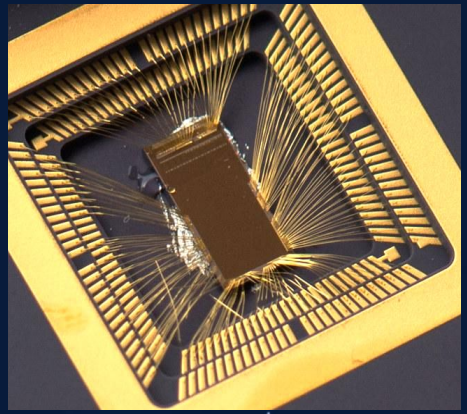
Global standards are a catalyst to accelerate technical innovation

Standards have been critical to technology innovation, adoption, and growth for decades

Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community

RISC-V is an Open Standard Instruction Set Architecture (ISA)

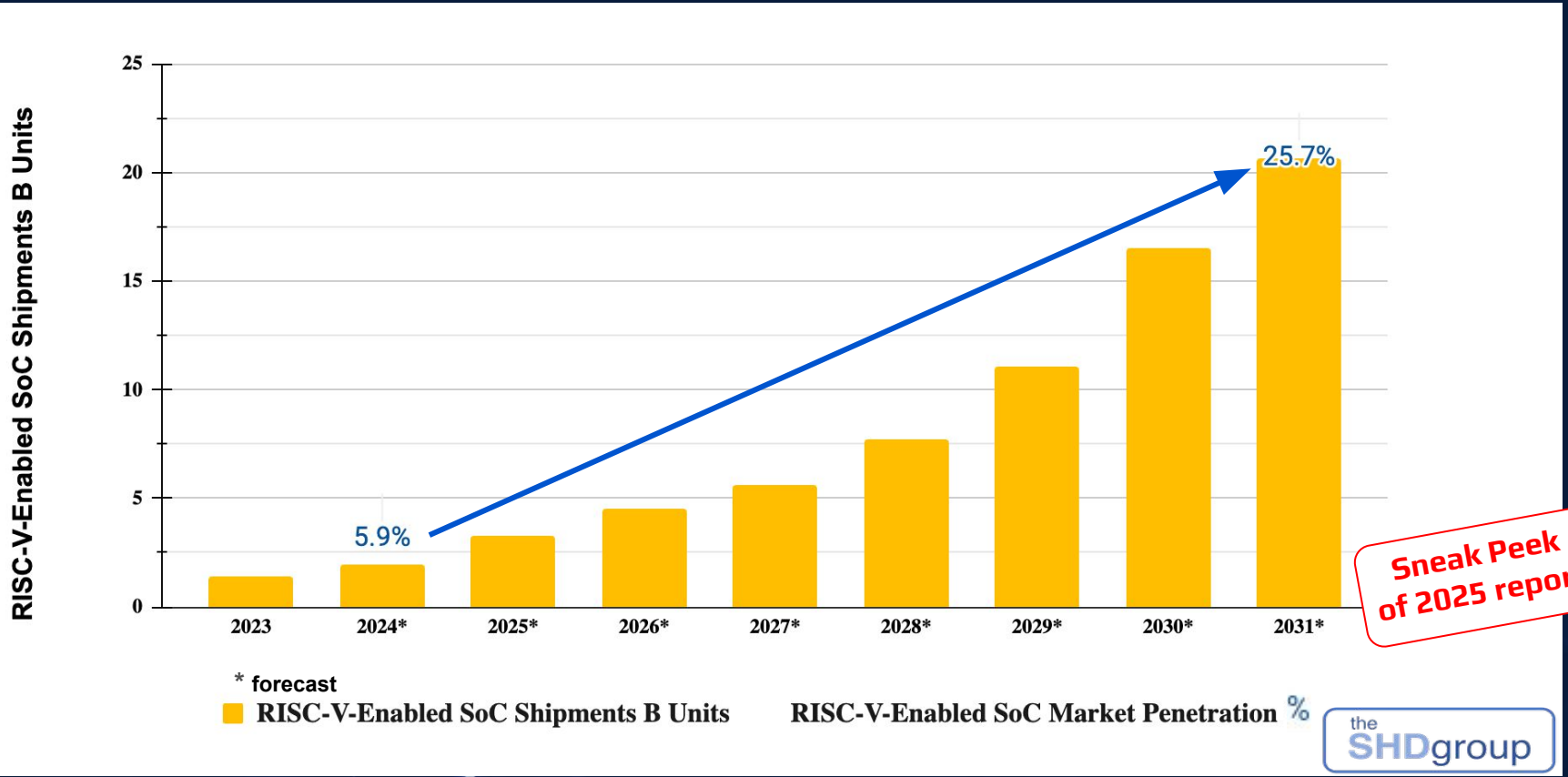
Software uses the ISA to tell the hardware what to do.

The RISC-V ISA and extensions ratified by RISC-V International are royalty free and open base building blocks for anyone to build their own solutions.

RISC-V International is the global non-profit home of the RISC-V ISA, related specifications, and stakeholder community

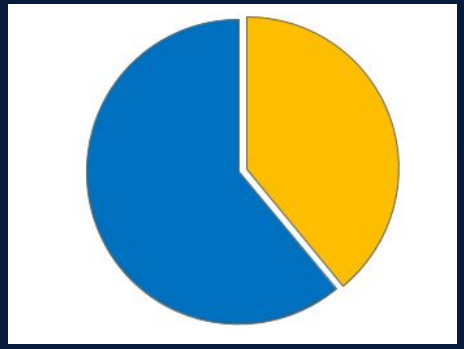
Incredible Market Potential

20B RISC-V SoCs, to Surpass 25% of Market

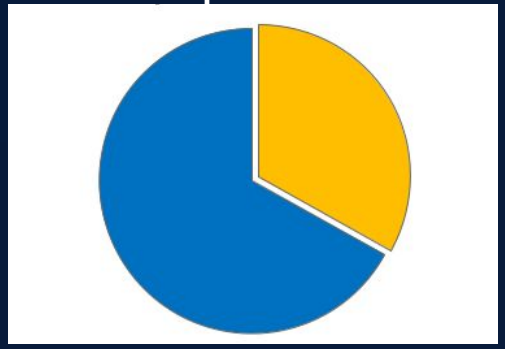


Top Markets for RISC-V 2031

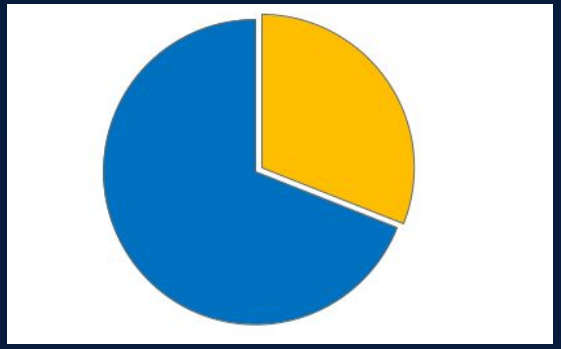
Consumer: 39%



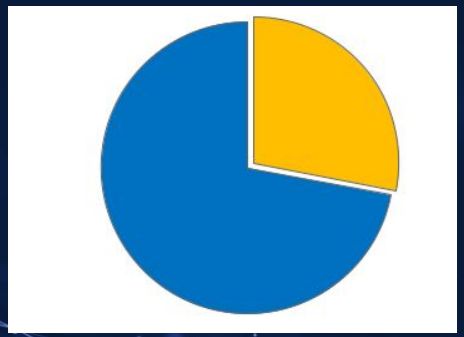
Computer: 33%



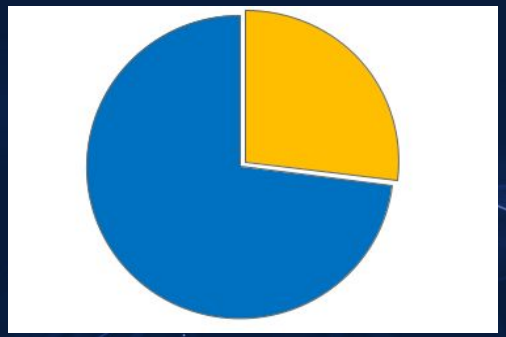
Automotive: 31%



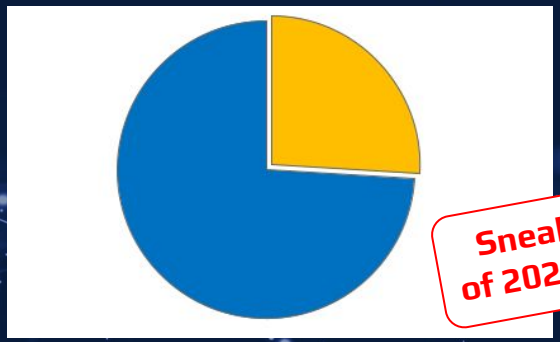
Data Center: 28%



Industrial: 27%



Networking: 26%



Sneak Peek of 2025 report

Source: The SHD Group October 2024

RISC-V

the SHDgroup

The technical foundation for lasting success

Countries

- Tech sovereignty
- Accelerate local innovation and talent
- Incubate technology ecosystem from research to industry
- Access worldwide market

Multinationals

- Control strategic roadmap
- New opportunities for innovation and influence
- Growth business models
- Avoid vendor lock-in

Researchers

- Collaborative ISA thought leadership
- Enables innovative research
- Access global RISC-V research network
- Tech transfer addressing real world applications

Startups

- Supercharge hardware and software co-design
- Accelerate strategic roadmap in greenfield applications
- Collaboration partners

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Opportunities and challenges with HPC

Software

- HPC workloads run on thousands of machines
- Different toolchains and programming models among CPUs, GPUs and accelerators
- Proprietary APIs from each vendor

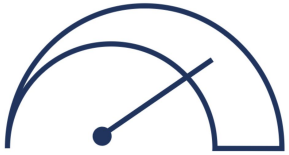
Processing

- Heterogeneous architectures with powerful multi-core CPUs, GPUs, custom accelerators
- Compute-bound vs memory bandwidth bound
- Cost and risk of changing to a new architecture

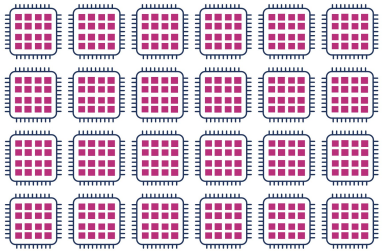
AI

- HPC is the foundation for scientific computing and machine learning
- The line between HPC and AI is blurring
- Doing AI at best helps HPC

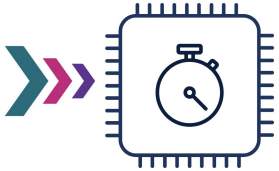
RISC-V Addresses the Requirements of HPC



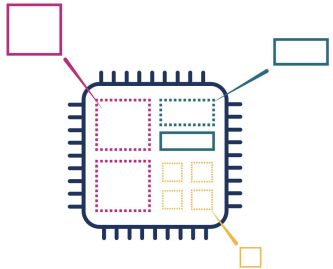
Compute architecture with a high level of performance



Ability to connect many processors running at the same time



HPC compute must not be memory bound



Compute customization for specific workloads

RISC-V is building the future of HPC through customization and open compute

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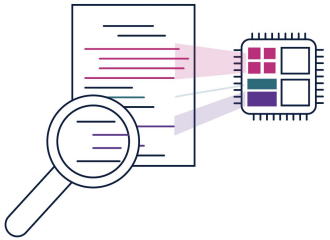
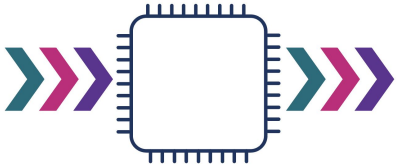
Customization



RISC-V enables specific compute blocks to be developed for specific workloads

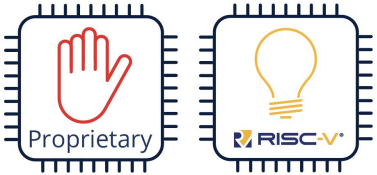
Start with a basic CPU the add extensions



RISC-V customization can add new flexibility and performance to memory access

Enables innovation, exploration, fast development and reusability

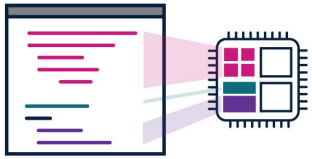
Open Compute



Openness creates diversity of innovation and more options

Valuable effort saved by pooling of resources

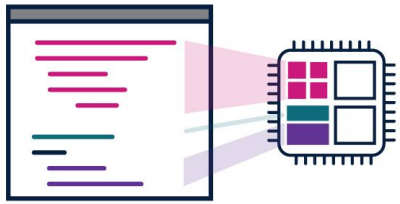
Sovereign compute initiatives can now develop HPC systems from scratch



Hardware / Software co-design innovation is accelerated

AI Specific, Custom Hardware Design

Extensible ISA enables a software-focused approach to AI hardware



Develop custom instructions and accelerators targeted at your software workload

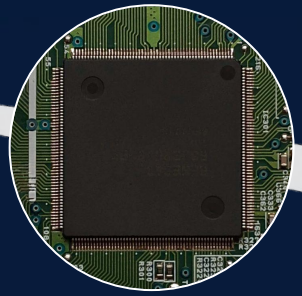
Unified programming model across AI workloads running on CPU, GPU & NPU

Latest advancements in AI/ML algorithms can be quickly integrated into hardware designs

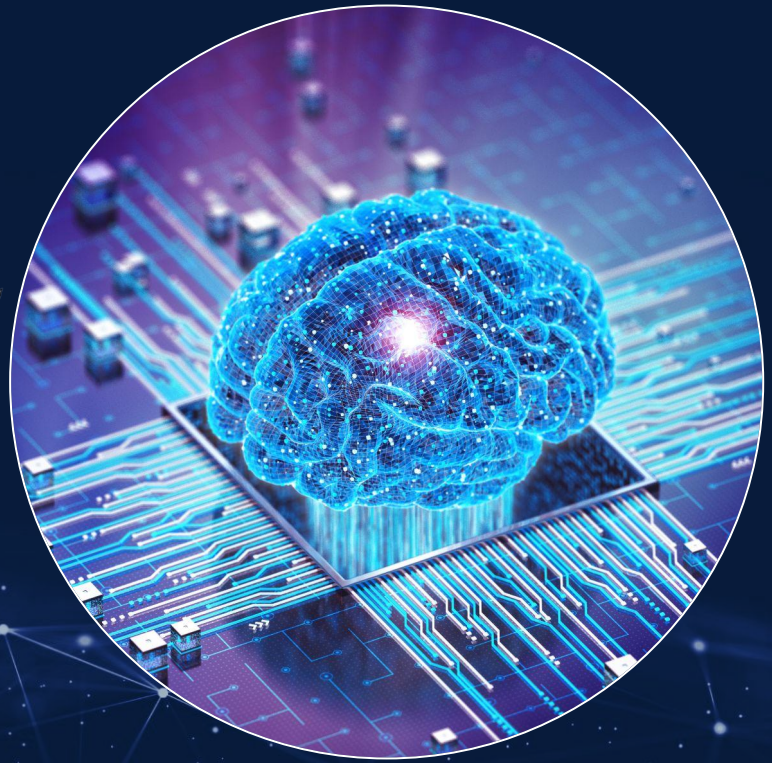
Entering the Era of Workload-designed Silicon

Mainframe

PC



SoC



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Profiles, Platforms and software ecosystem

Core ISA

ISA Extensions
Floating point,
Bit ops, Vector

non-ISA Extensions
Interrupt controller,
IOMMU

Software Extensions
Boot/Runtime Services
ABI Specification

Custom Extensions
Vendor specific

RVA
Application
Processor

RVB
Embedded
Processor

RVM
Microcontroller

Server

Mobile

Automotive

Embedded System

Edge AIoT/AI

Big Data, Database, LLM

Red Hat Enterprise Linux · Canonical Ubuntu · SUSE

Android Apps
Android

android

Android Auto
Safety Linux

Automotive Grade Linux

yocto PROJECT
Container runtime

Zephyr · freeRTOS

Extensions
Enable Diversity

Profiles
(mandatory ISA extensions)
Certainty for software

Platforms
(Profile + nonISA + software)
Certainty for OS & firmware

RISC-V

Main Specification Ratification in 2024

RVA23 Profile Ratified

Major release of RISC-V Application Processor Profile

Gives application compatibility across vendors

Major added extensions: Vector, Hypervisor

25 ratified specifications in 2024
Improving perf, security and resilience!

Performance

Quality-of-Service (QoS) Identifiers, Obviating Memory-Management Instructions after Marking PTEs Valid

Capacity and Bandwidth QoS Register Interface

Control Transfer Record

Zaamo and Zalrsc Extensions, Byte and Halfword Atomic Memory Operations

BF16 Extensions

Smcdeleg, Indirect CSR Access

Profiles

RVA23, RVB23

Security and Resilience

Priv 1.13, Pointer Masking

Double Trap, Resumable Non-Maskable Interrupts

Shadow Stacks and Landing Pads

May-Be-Operations

RERI Architecture

Functionality and debugging/Tracing

B Standard Extension for Bit Manipulation Instructions, Functional Fixed Hardware Specification, Supervisor Binary Interface 2.0, E-Trace Encapsulation, N-Trace, Trace Control Interface, Trace Connectors

6 ratified specifications in 2025
Improving perf, platform and debug

Performance

Load/Store Pair for RV32

RVV C Intrinsics

Profiles and platforms

Server SOC

IO Mapping Table (RIMT)

Debugging/Tracing

Debug for Hardware Platforms

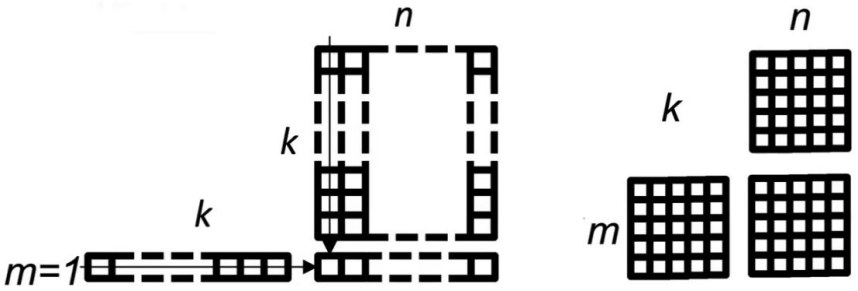
Semi-hosting

Main Target for 2025

2025: Main Specification Areas

- ✓ Vector C Intrinsics
- Matrix extensions for AI and HPC
- Security for Confidential Compute, memory safety
- ✓ Server SoC and Server Platform

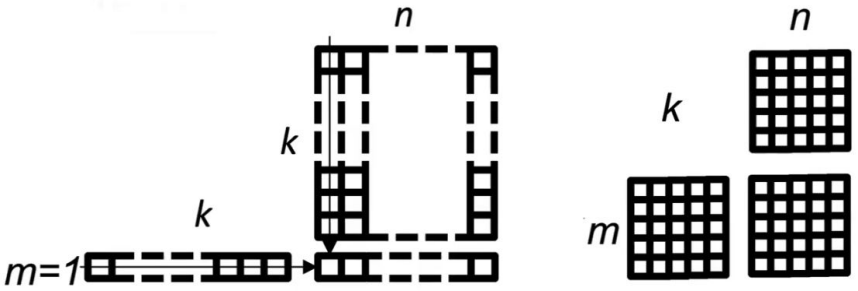
Matrix Extensions: Inner vs Outer product



Inner Product

- Multiply one element of a row with the corresponding element of a column one-by-one and accumulate the products as they are computed

Matrix Extensions: Inner vs Outer product



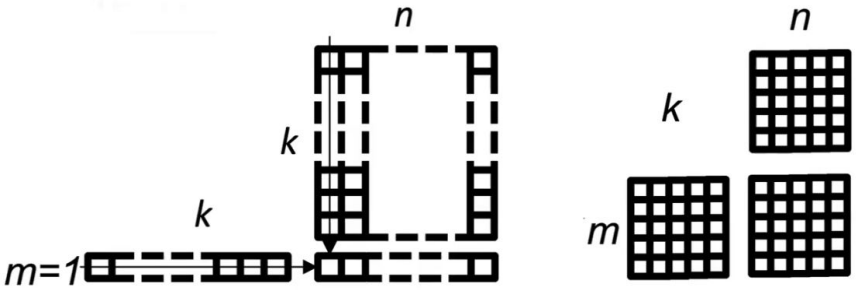
Inner Product

- Multiply one element of a row with the corresponding element of a column one-by-one and accumulate the products as they are computed

Outer Product

- Multiply all elements of one row with the corresponding elements of a column in parallel
- Sum all the intermediate products

Matrix Extensions: Inner vs Outer product



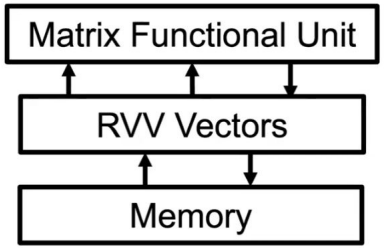
Inner Product

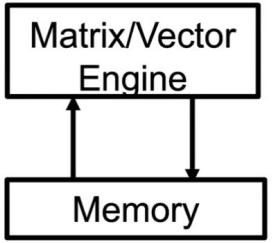
- It can be easily computed by adding a simple new vector dot product instruction

Outer Product

- It can be implemented by adding new status registers to hold the intermediate products and new dedicated matrix instructions

Matrix Extensions: with or without RVV





RVV RISC-V Vector Extension

1. Vector dot product for inner product
2. Build matrix operations and instructions on top of the existing RVV extension
3. Build matrix operations independently of RVV

Considerations: die size, latency, throughput, mixed vector and matrix operations, one matrix unit per core or one larger matrix engine shared across multiple cores

Unify the integration in ML frameworks → MLIR IREE, TVM back-end, ONNX EP, etc.

RISC-V®

Building the strongest software ecosystem

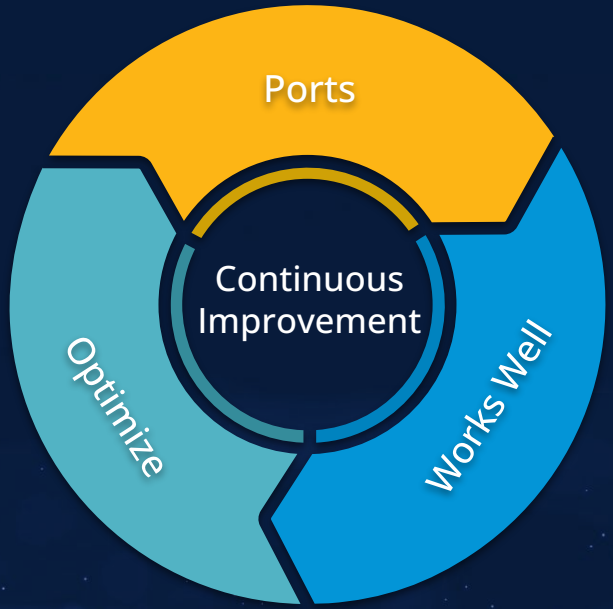
landscape.riscv.org

RISC-V Software Ecosystem project

- Compilers
- Toolchains
- System libraries
- Kernel
- Virtualization
- Programming languages
- Linux distribution integration
- Tools for debug and profiling
- AI/ML

+

Iterative Improvement in Software Porting and Optimization



Ports	Functional porting to new ISAs
Works Well	Refinements to improvement on performance and efficiency
Optimize	Algorithmic Optimization Architecture Specific Optimization

RISE
RISC-V Software Ecosystem

Example of Software Invested Projects by RISE

Check out the RISE Wiki: https://wiki.riseproject.dev/

RISE
RISC-V Software Ecosystem

Resources

Testbeds available from

- HCA testbed (Barcelona Supercomputing Center - BSC)
- EPCC (University of Edinburgh)

RISC-V HPC SIG https://lists.riscv.org/g/sig-hpc

RISC-V HPC Market Development Group: https://lists.riscv.org/g/mktdev-hpc/

Powering the Future of High Performance Computing? Nick Brown, RISC-V Summit EU 2025 Paris

HPC Keynote panel at the RISC-V Summit North America 2024 with Luisa Gonzales, Nick Brown, Travis Lanier, Wei-Han Lien, Andrew Moore

RISC-V@BSC: Fostering RISC-V strategy in the EU through Research, Innovation & Education by Teresa Cervero

Performance characterisation of the 64-core SG2042 RISC-V CPU for HPC by Nick Brown and Maurice Jamieson

Accelerating stencils on the Tenstorrent Grayskull RISC-V accelerator by Nick Brown and Ryan Barton

RISC-V ISA and Ecosystem

Your Innovation