Pilot using Independent Local & Open Technologies

The European PILOT

ISC24 – International RISC-V Workshop

Carlos Puchol, BSC – May, 2024

The European PILOT project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No.101034126. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Italy, Switzerland, Germany, France, Greece, Sweden, Croatia and Turkey.

Overview

Project Information

The European PILOT

Grant agreement ID: 101034126

Start date
1 December 2021

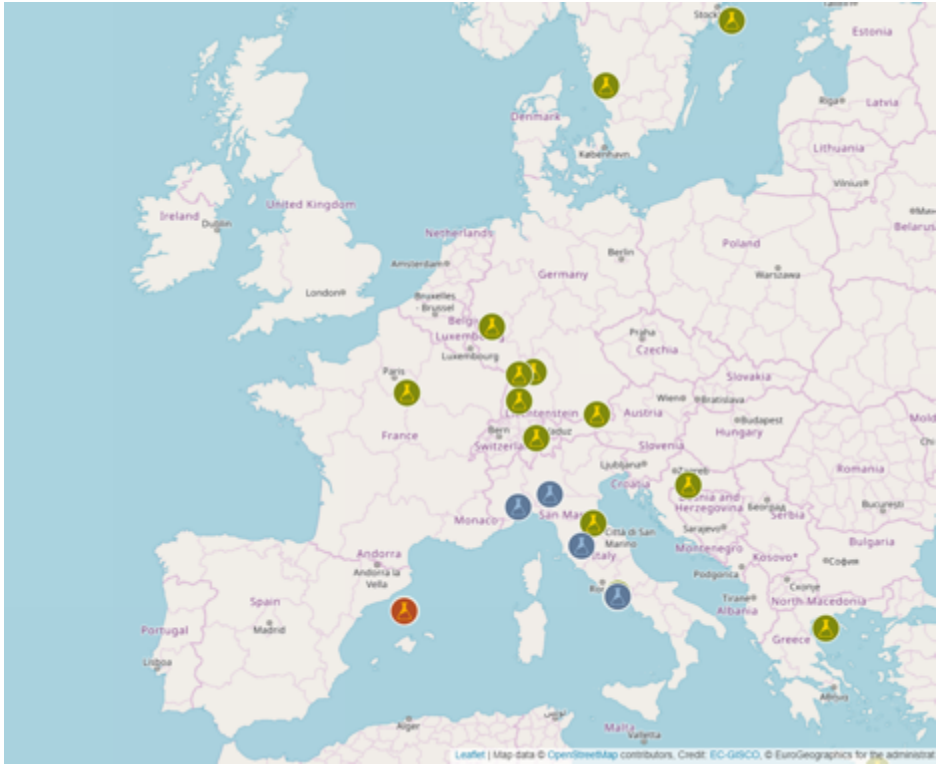
End date
31 May 2025

Funded under
H2020-EU.2.1.1.
H2020-EU.2.1.1.2.

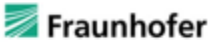
Overall budget
€ 29 999 925

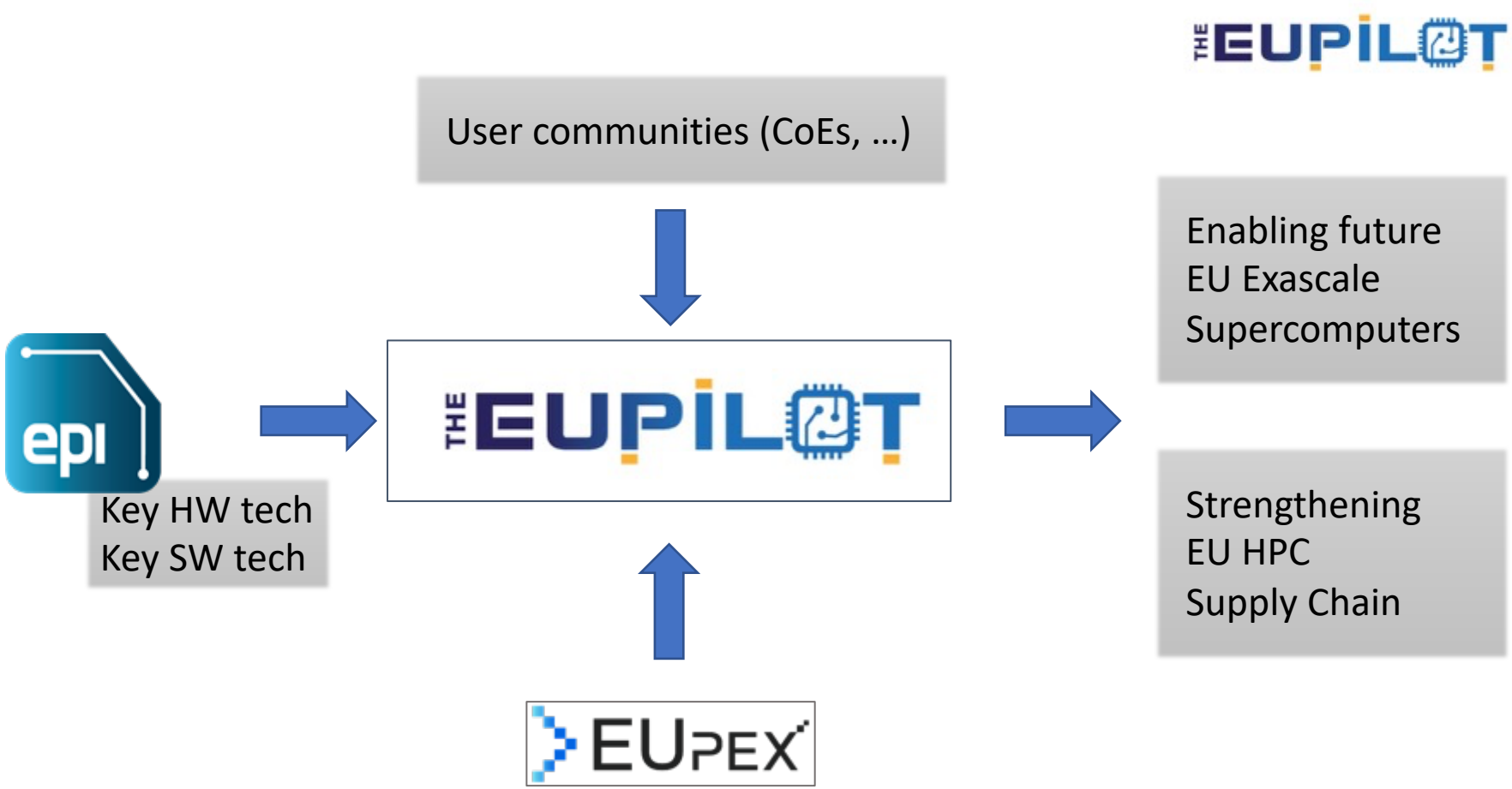
EU contribution
€ 14 999 962,51

Coordinated by
BARCELONA SUPERCOMPUTING CENTER-CENTRO NACIONAL DE SUPERCOMPUTACION
Spain



Consortium: 19 Partners




THE EUPILOT
User communities (CoEs, …)
epi
Key HW tech
Key SW tech
THE EUPILOT
Enabling future
EU Exascale
Supercomputers
Strengthening
EU HPC
Supply Chain
EUPEX

Objectives

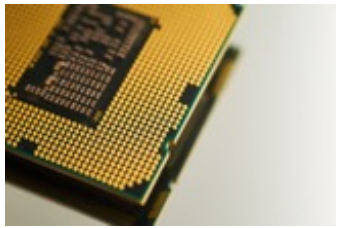
➔ **Demonstrate a European pre-exascale accelerator platform**

- Design, validate, build and deploy a fully-integrated accelerator platform
- Maximize use of European technology & assets
- Stimulate European collaboration, enable future exascale systems
- Co-design, for improved performance and energy efficiency
- Leverage & extend open source and RISC-V into HPC

➔ **Strengthen European digital autonomy and HPC supply chain**

Target: Chips → Deployments

- **Hardware** Chips → Modules → Boards
- **Systems** Boards → Systems → Liquid Immersion Deployments
- **Software** Drivers → OS → Compilers → Frameworks → Apps



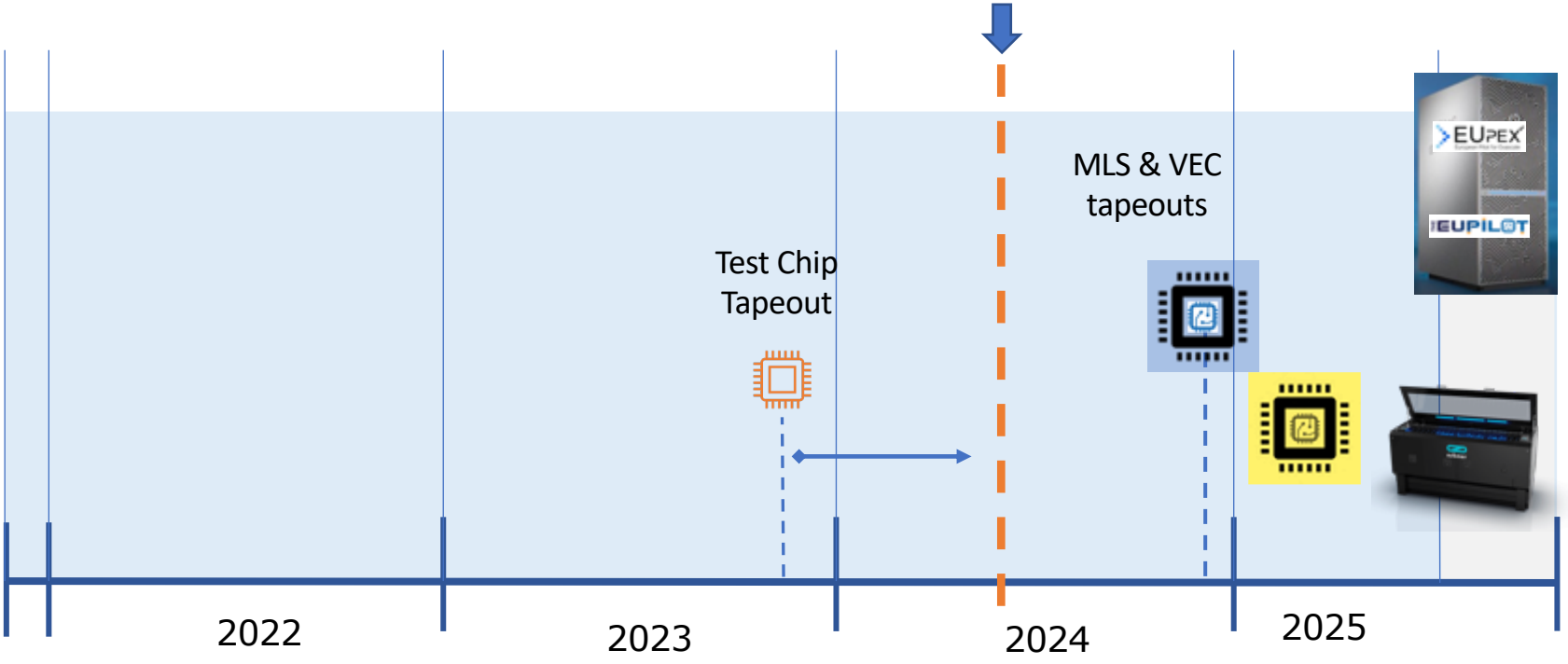
Target: Chips → Deployments

- **HW accelerator efforts built upon key IPs from EPI-SGA1 project**
- **Tape-outs: from 22nm → 12nm**
  - One test chip
  - Two accelerator chips: one VEC & one MLS
- **Target HPC (VEC) and HPDA (MLS) applications**
  - Port apps/frameworks/libraries to RISC-V
  - Develop toolsets for manual or automatic optimizations
- **Deploy OCP based systems to datacenter with liquid immersion cooling tanks**
  - Higher workloads, density & capacity
  - Reduced environmental impact

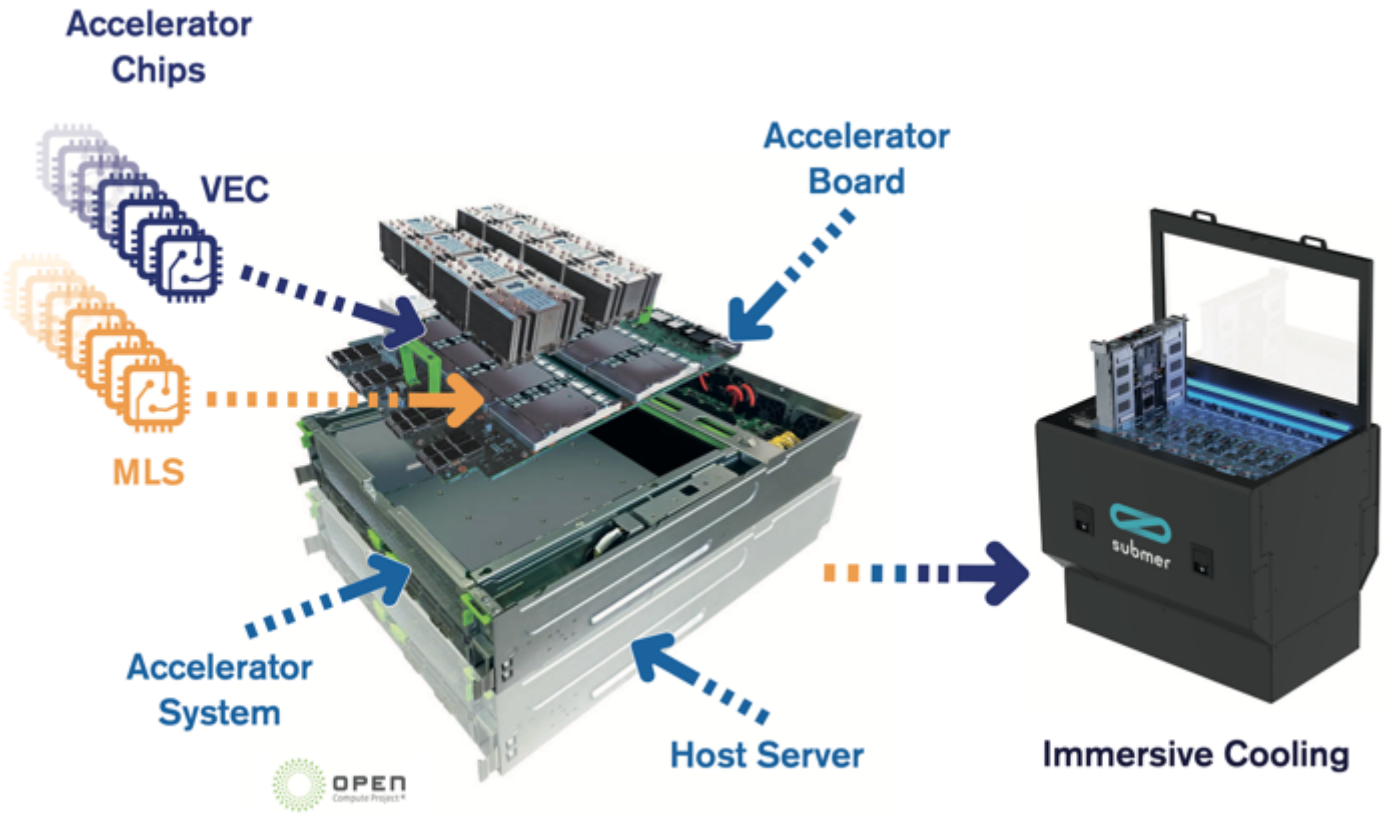
- **Goal: deploy EUPILOT *demonstrator* accelerators in MN5 environment**
- **Reach: seed SDV for later supercomputer projects**

Timeline*

(You are here)

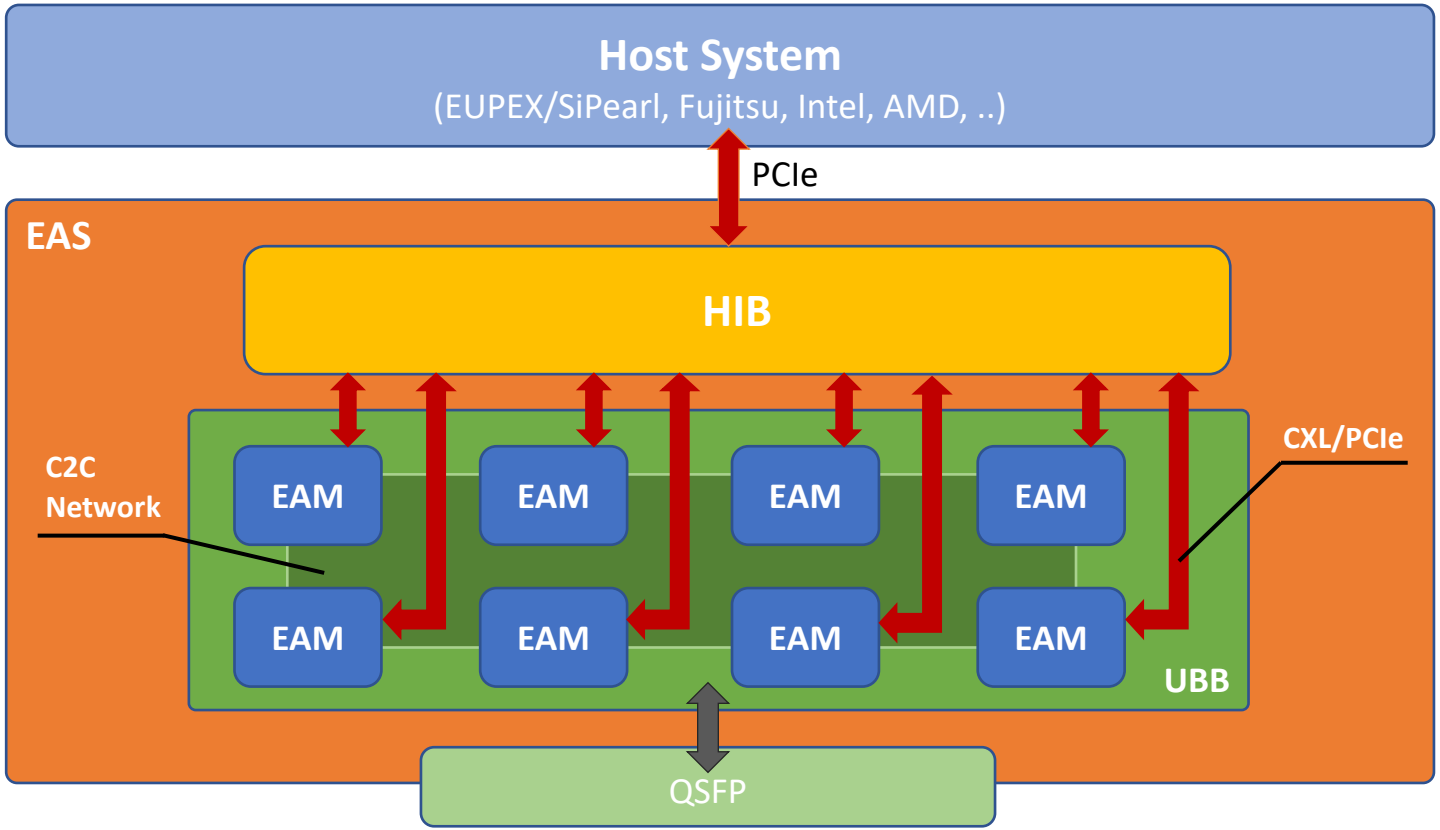


Top Level View

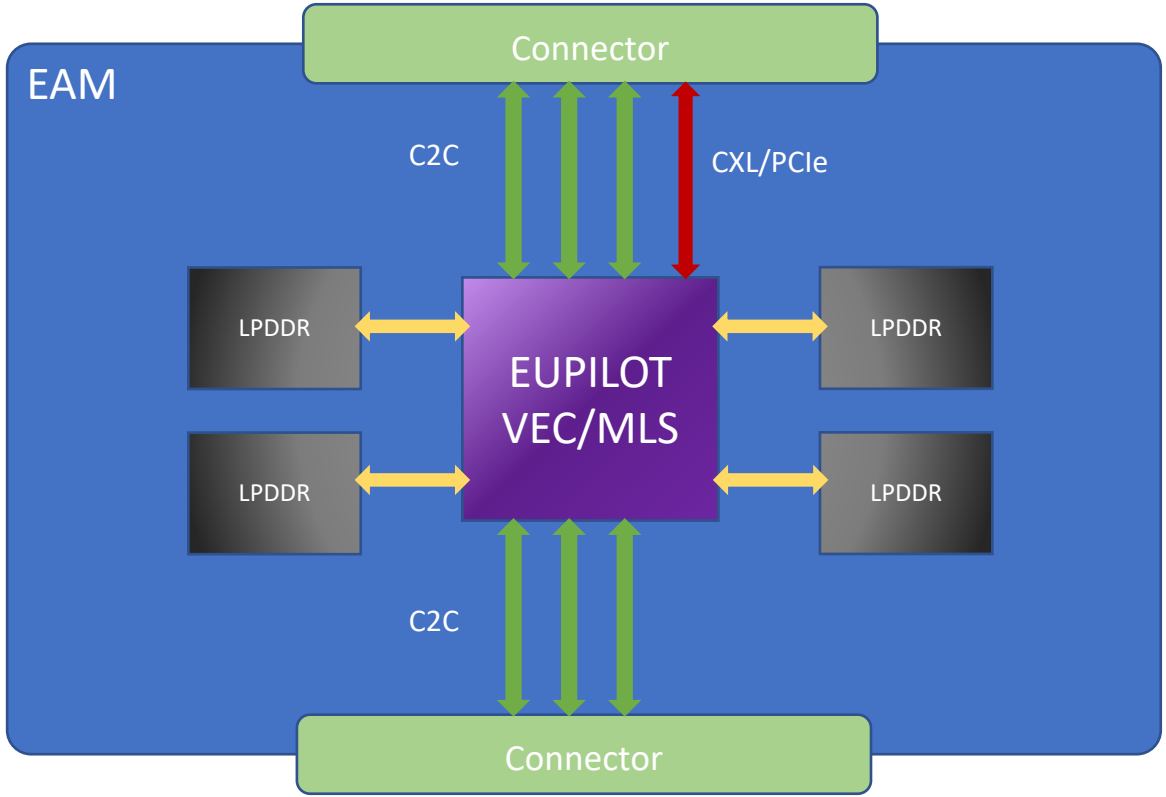


EUPILOT System Architecture

EUPILOT Accelerator System



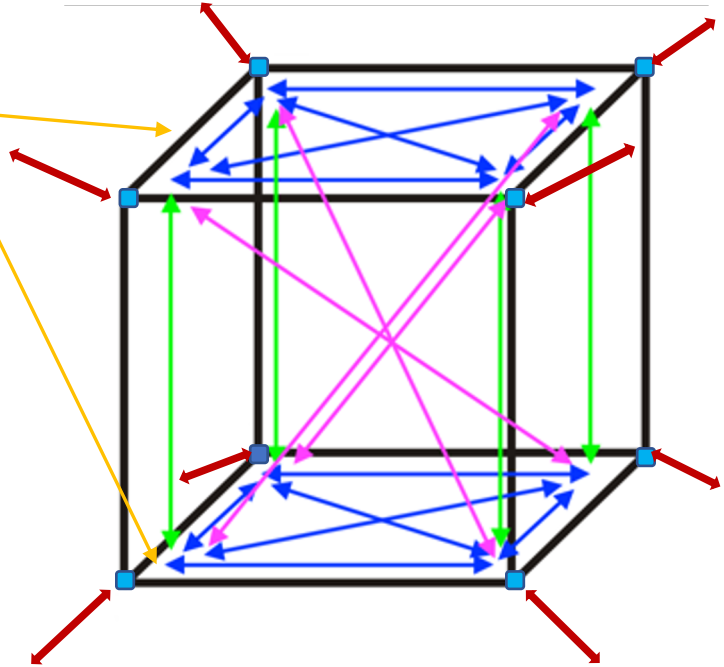
EAM – EUPILOT Accelerator Module



EAMs "Dual-quad" Interconnects

Two fully-connected EAM quads with

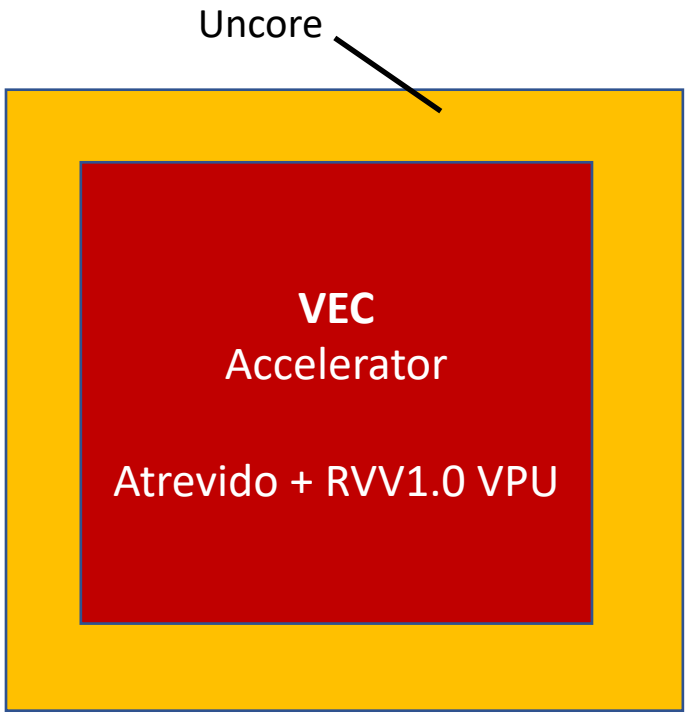
- Two-link interconnects
- Coherent memory



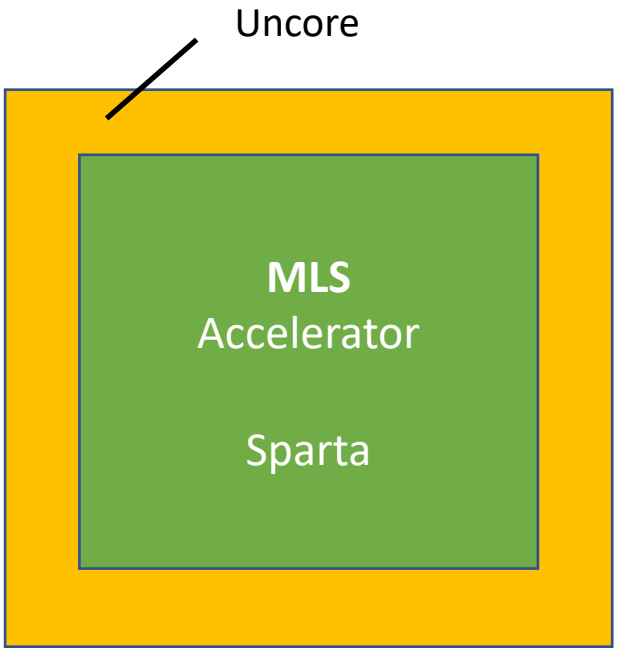
To/from QSFP

(scale-out configurations)

Accelerator Chips



48~54 mm²

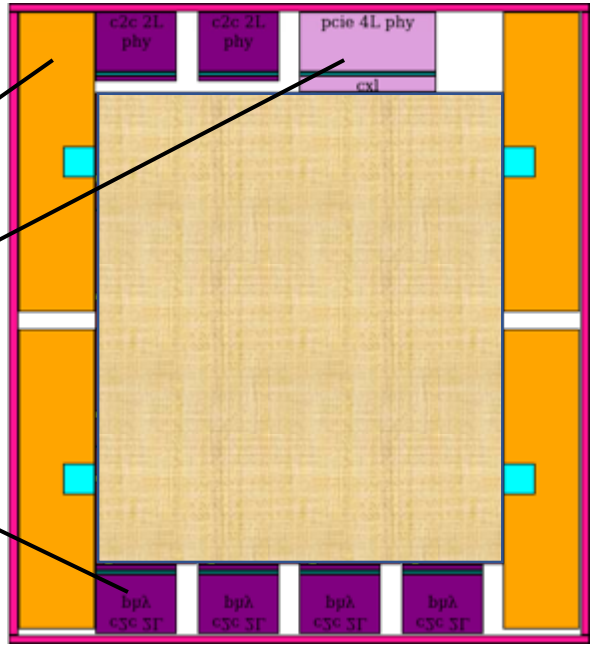


~40 mm²

12nm GlobalFoundries 12LP+ process

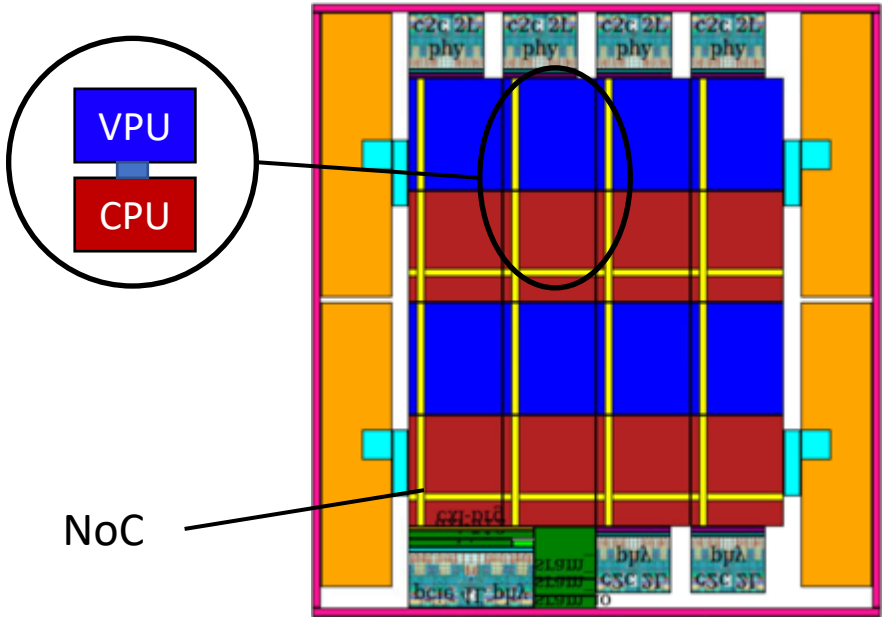
Common/reusable Uncore

- **Reusable uncore to VEC/MLS chips, others**
  - Reuse most of the layout
  - Compatible footprint to reuse EAMs
- **4 x LPDDR controller and PHYs**
- **1 x CXL 4-lane controller and PHY**
- **6 x C2C 2-lane controllers and PHYs**

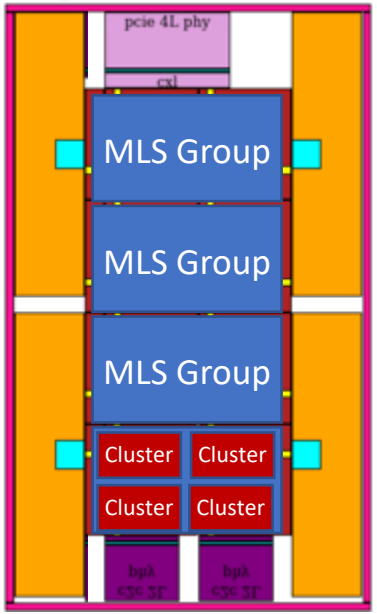


Shown above with VEC Layout

EUPILOT Planned Die Layouts

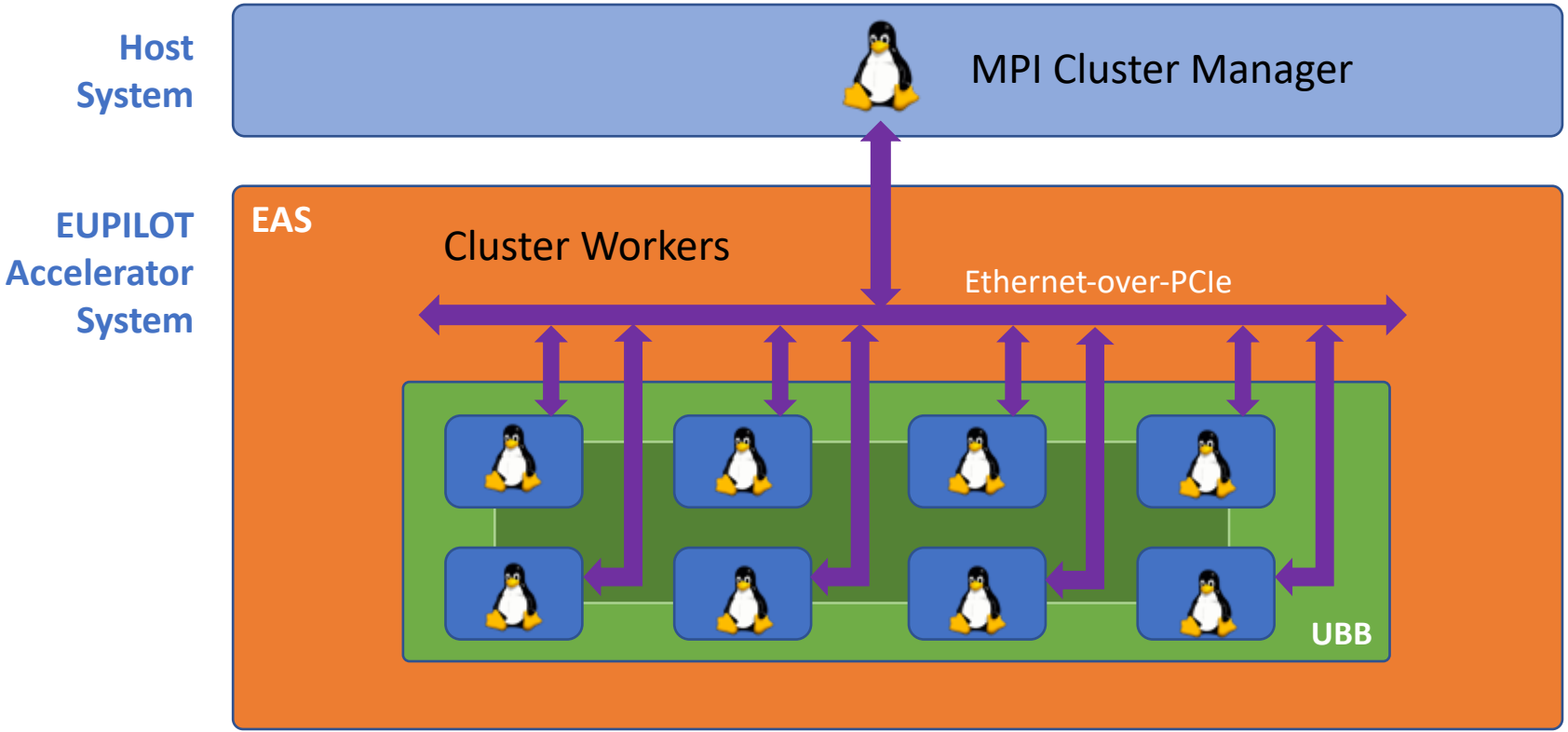


VEC

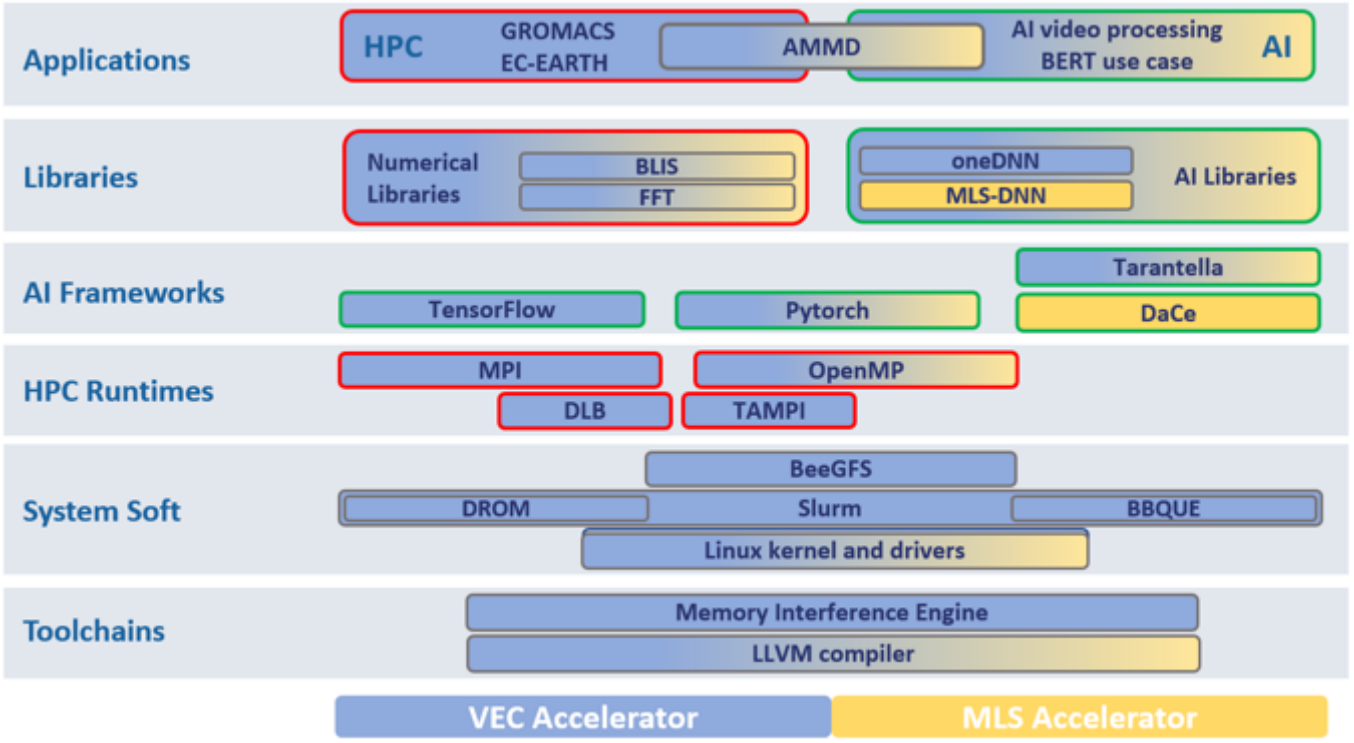


MLS

(VEC) Software Architecture



Software Stack



Thank you!

www.eupilot.eu

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