Enabling energy-efficient architectures

Fourth International workshop on RISC-V for HPC

Karel Masařík Ph.D.
RISC-V International BoD member
Codasip President & Founder

Hamburg, May 16th, 2024

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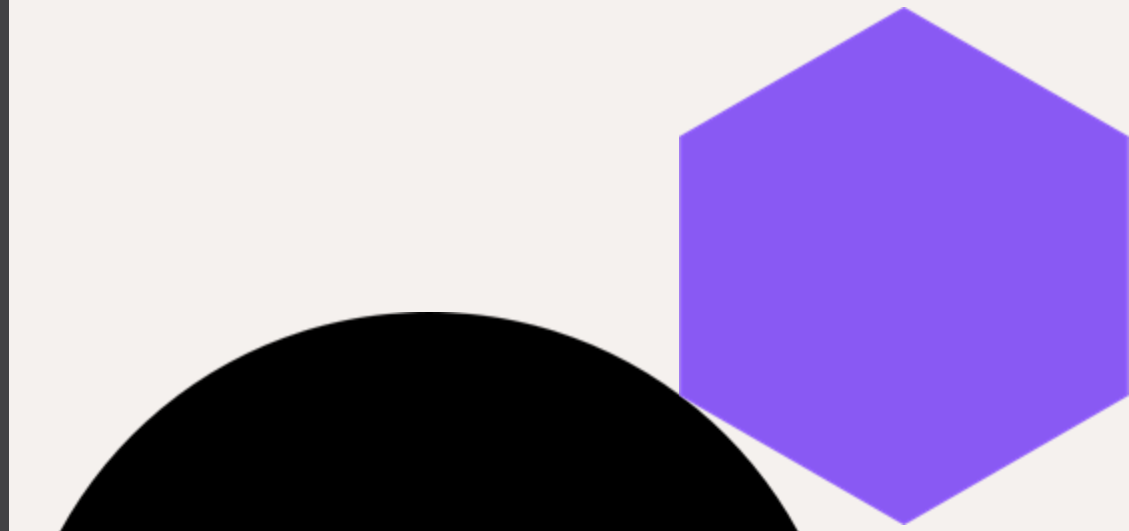

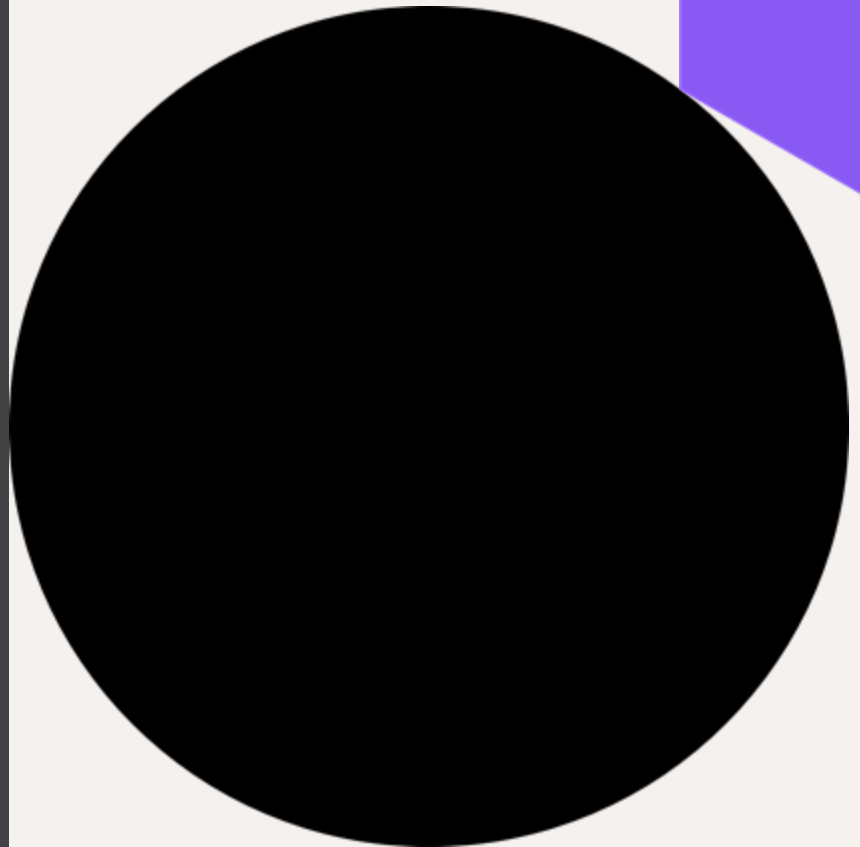

The Custom Compute needs in HPC

→ HPC Significant changes

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Generative AI is a near-term game changer

Computing on the edge supporting real time decision making

End user decisions for on-premises vs cloud vs hybrid

Quantum computing is evolving

→ One size no longer fits all

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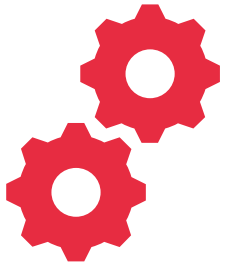
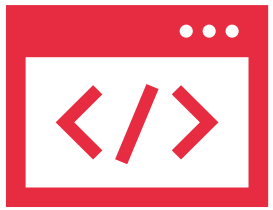


Diverse workload is making the HPC system more complex

Variety of workload = variety of the architectures

- Processors: x86, ARM, RISC-V
- Accelerators: Nvidia Grace Hopper, AMD MI300, Graphcore, etc.



Moving from monolithic architectures towards more flexible, heterogenous designs that are based on chiplets

→ Arm-based HPC system revenues expected to more than triple by 2027

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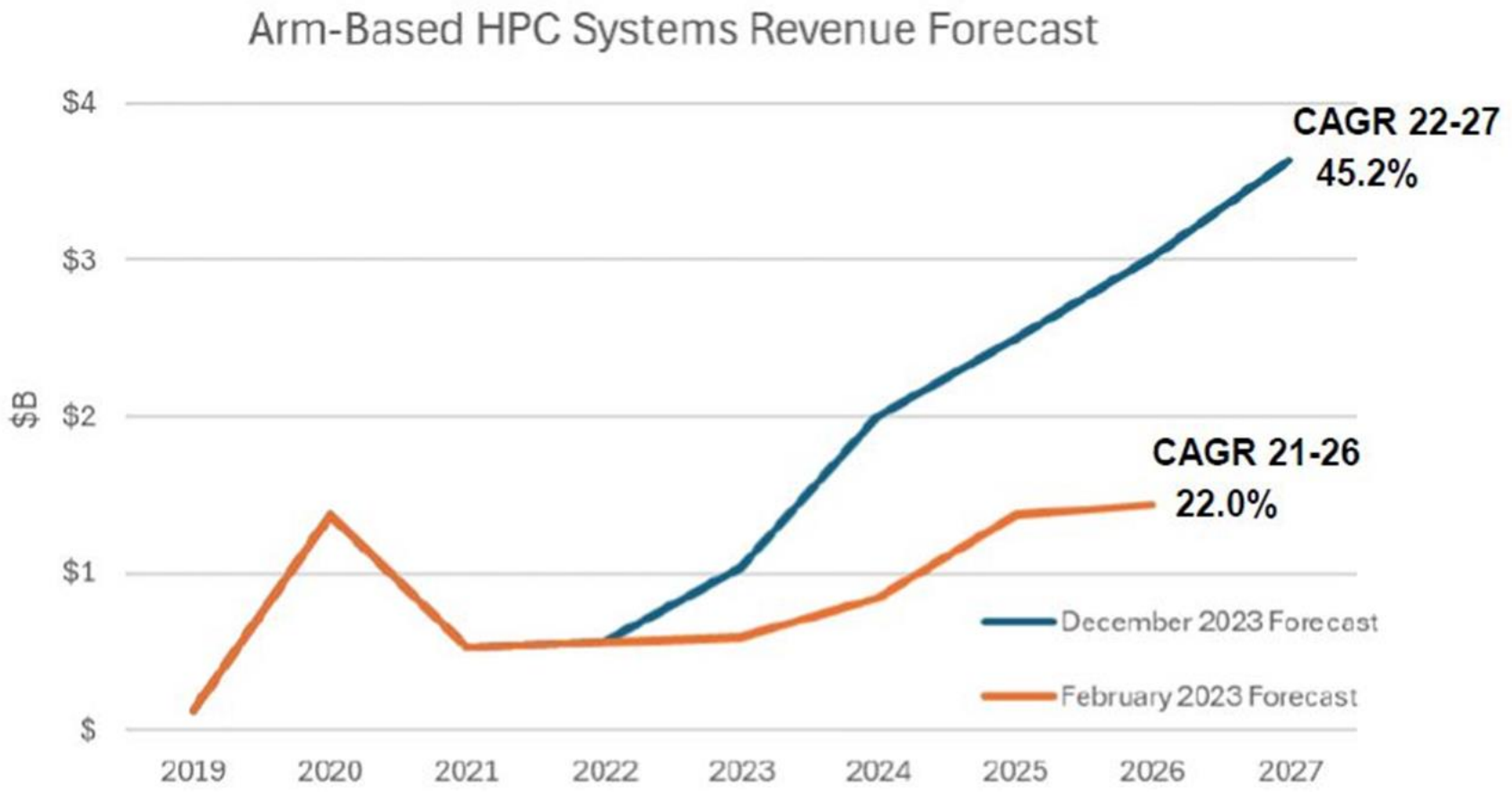
Arm-based on-premises HPC sever market forecast increased significantly due to increased optimism about Arm HPC adoption and expanding scale*



*Hyperion Research 2024

→ Sustainability in Procurement

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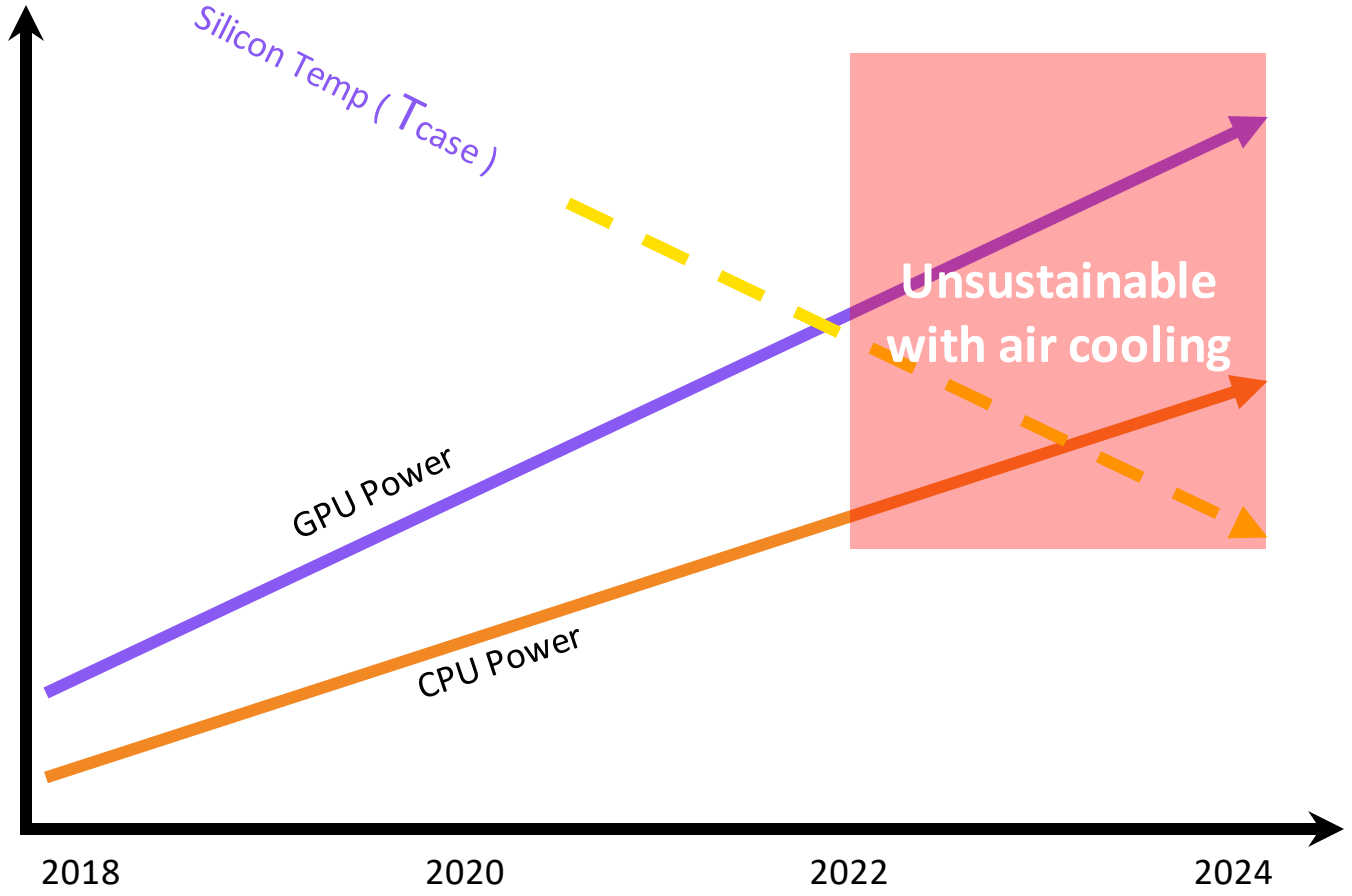
- Sustainable and energy efficient solution main factor in the procurement
  - Caused by energy crisis, inflation and geographical concerns
- Energy consumption legislation being formed
  - Energy-aware procurement
  - Renewable energy/where possible
  - Optimizing workload for efficiency
- New technologies are needed for improvement energy usage

→ More technical challenges: The Cooling

- Power per device increasing exponentially
  - Expecting devices up to 1000 Watts in next years
- Maximum allowable temperature coming down



→ Enabling energy-efficient designs via Custom Compute with RISC-V architectures

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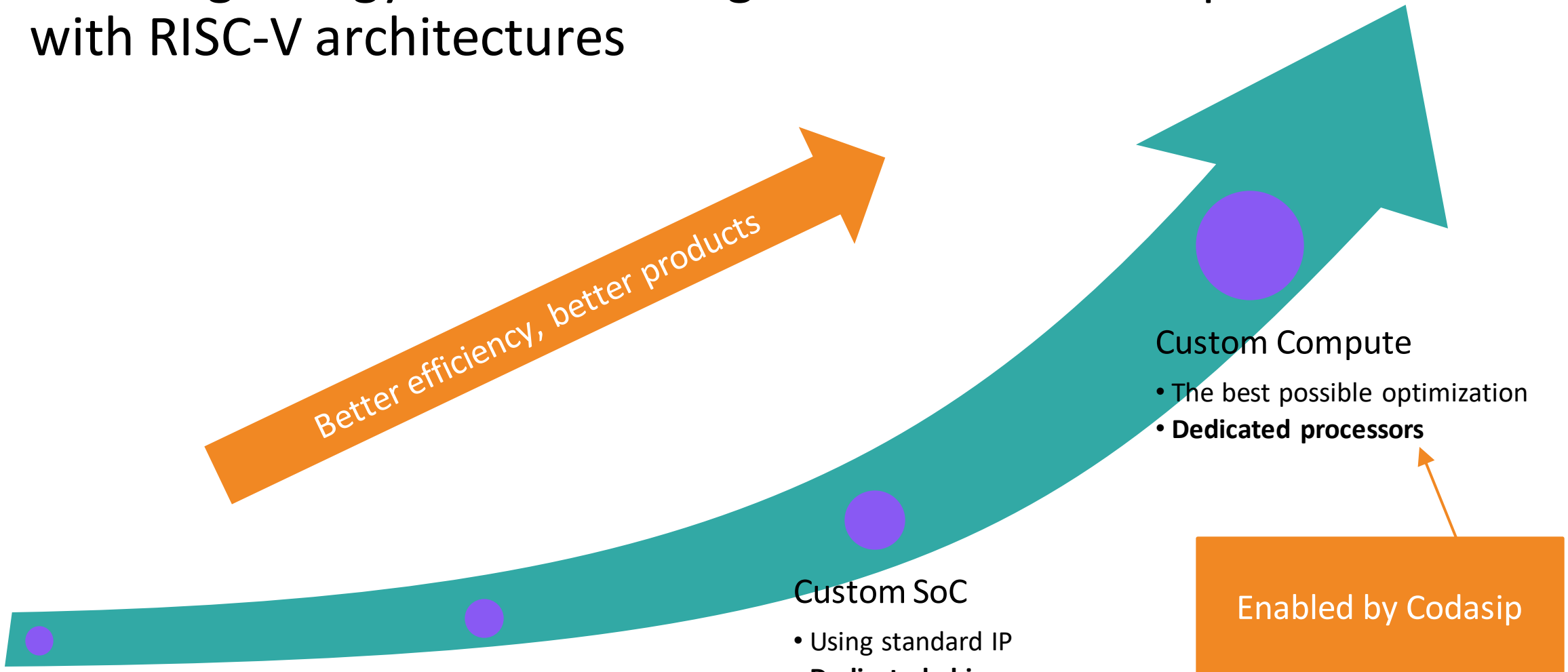
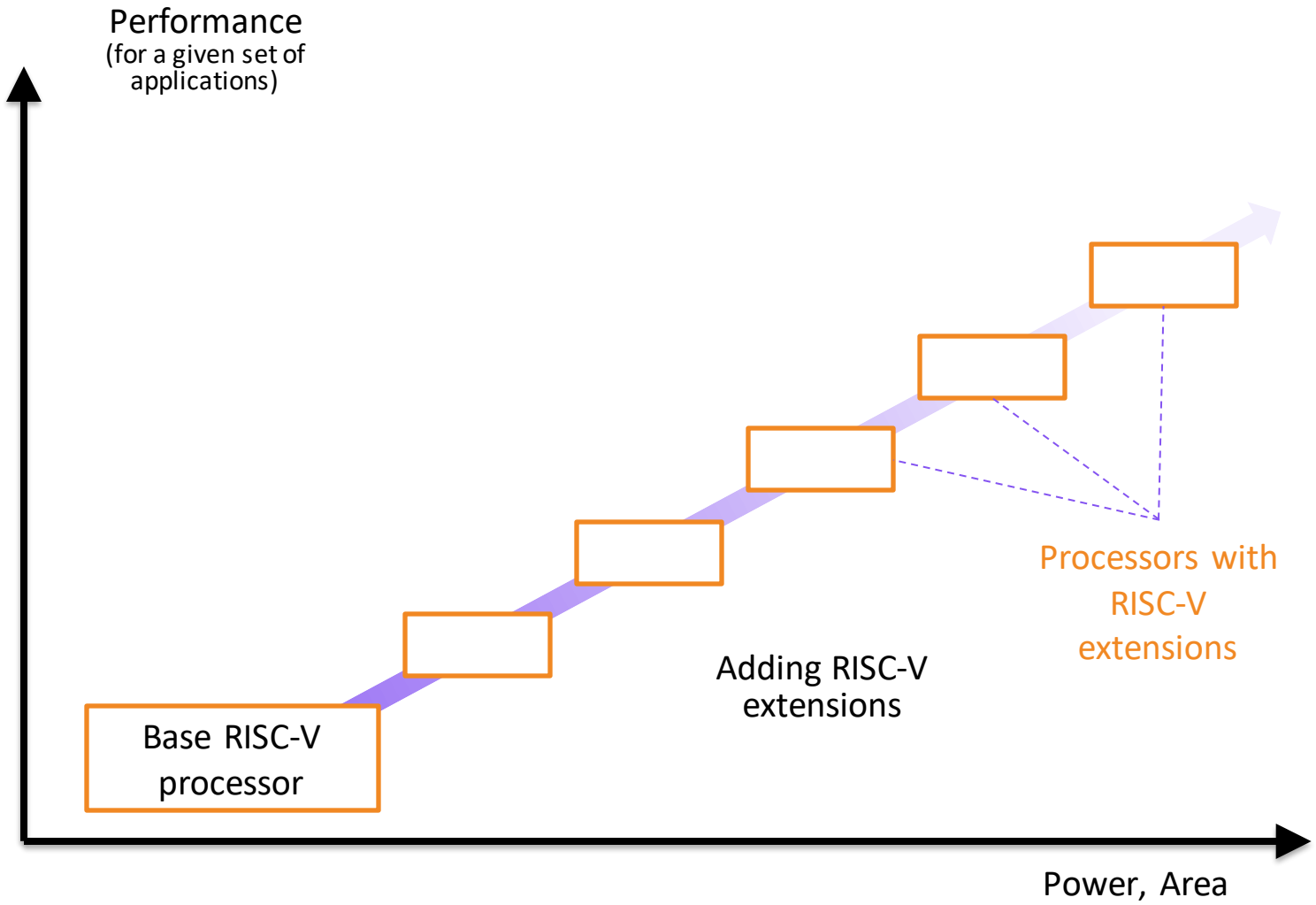
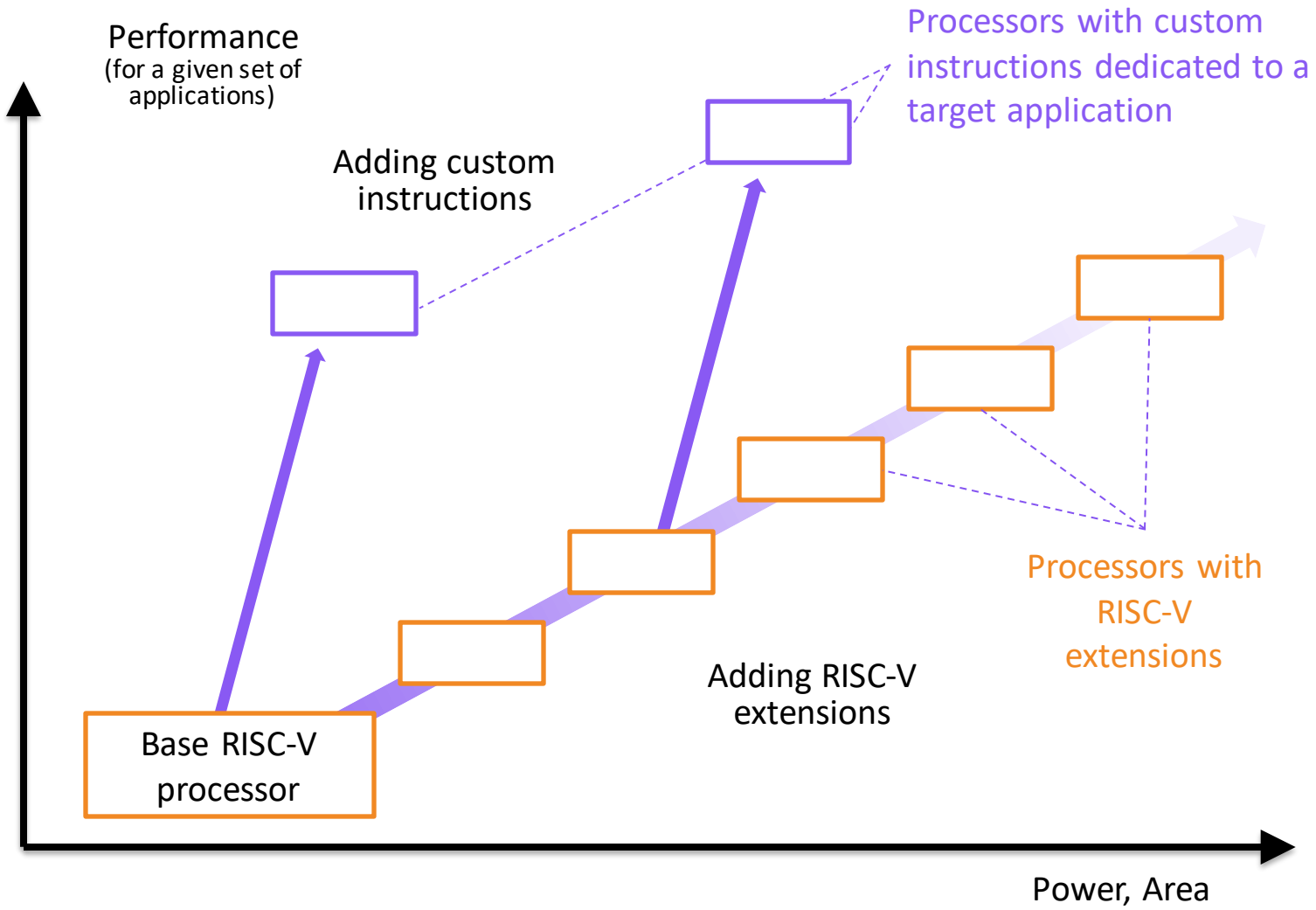


→ RISC-V extensions give flexibility



- RISC-V is modular
- Base is minimal
- Extensions target specific application

→ RISC-V Custom Instructions enable efficiency



- RISC-V allows custom instructions
- Optimally designed for target application

→ Custom Compute

→ Custom Compute is usable everywhere

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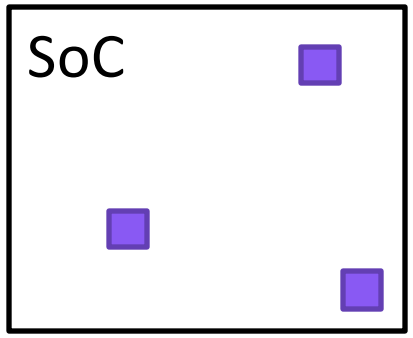
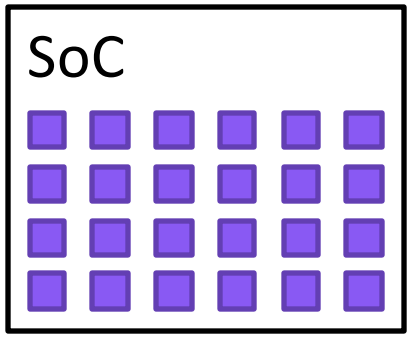
Optimized embedded cores



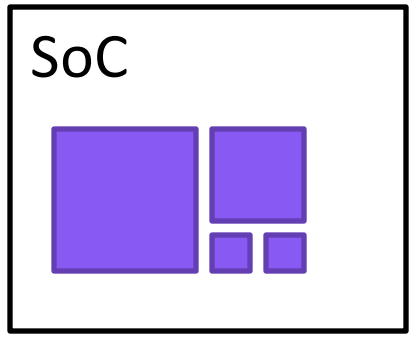
- System management
- Power control
- Security
- …

Specialized cores



- AI
- Systolic array engines
- In memory compute
- …

Heterogeneous compute

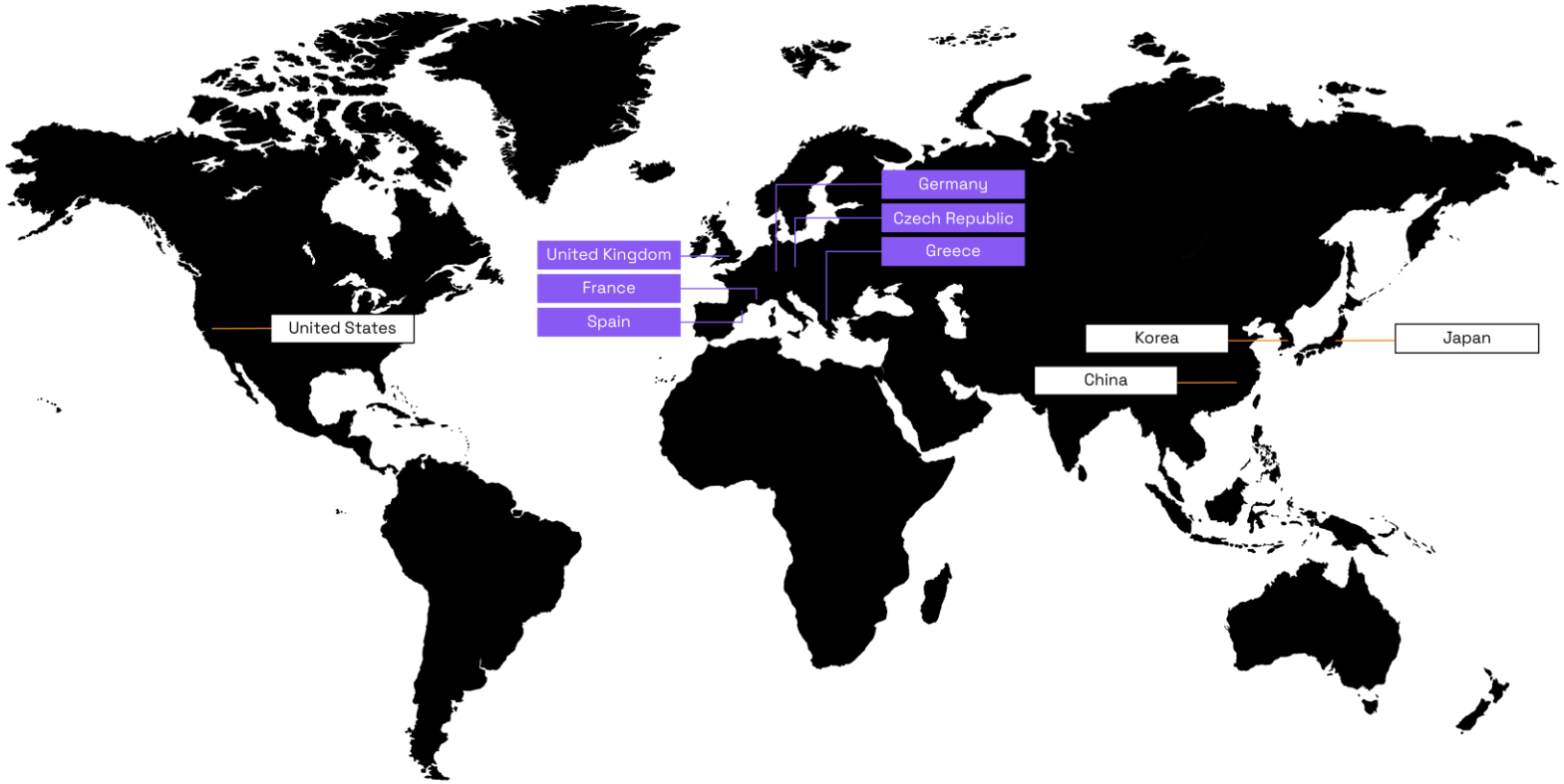


- Optimized main CPU
- Vector/tensor engines
- DSP, VLIW
- GPU
- …

Codasip in brief

→ Codasip overview

- Founded in 2014
- HQ in Munich
- More than 250 employees
- Design teams in Europe
- Processor solution company
- RISC-V® co-founder
- Leading Custom Compute



→ Senior Leadership Team

Ron Black

Chief Executive Officer

Over 25 years running software and semiconductor businesses in Europe and the US, including microprocessor and IP licensing businesses. He specializes in corporate transformations and has a history of significant exits.

Zdeněk Přikryl

Chief Technology Officer

Over 15 years of experience in processors design from small MCUs to complex DSPs/VLIWs, embedded systems design, HLS, simulation, driving R&D.

Simon Bewick

VP IP Engineering

Over 30 years designing and delivering SoC devices to volume production, managing development teams from architecture through to silicon qualification and operating across multiple locations and geographies.

Kateřina Smrčková

Chief People Officer

Over 10 years of HR experience in international companies, both big and small. All-round HR expertise. Personal motto: Making Codasip a happy place to work and grow.

Karel Masařík

Founder & Head of Labs

Over 20 years in processor development and design tools. Founded Codasip based on his PhD thesis and currently leading Codasip's innovation initiatives.

Vladimír Koutný

Chief Financial Officer

Over 15 years of experience in high-growth technology companies. All-round financial and operational expertise.

Jamie Broome

VP Product Management & Automotive

25 years leading the full IP product and engineering life cycle for complex processors and SoC systems. GPUs, CPUs, connectivity, and accelerator/AI systems.

Brett Cline

Chief Commercial Officer

Over 25 years of leadership experience in sales, marketing, and engineering. Proven methodology for growing sales. Involved with seven company mergers/acquisitions.

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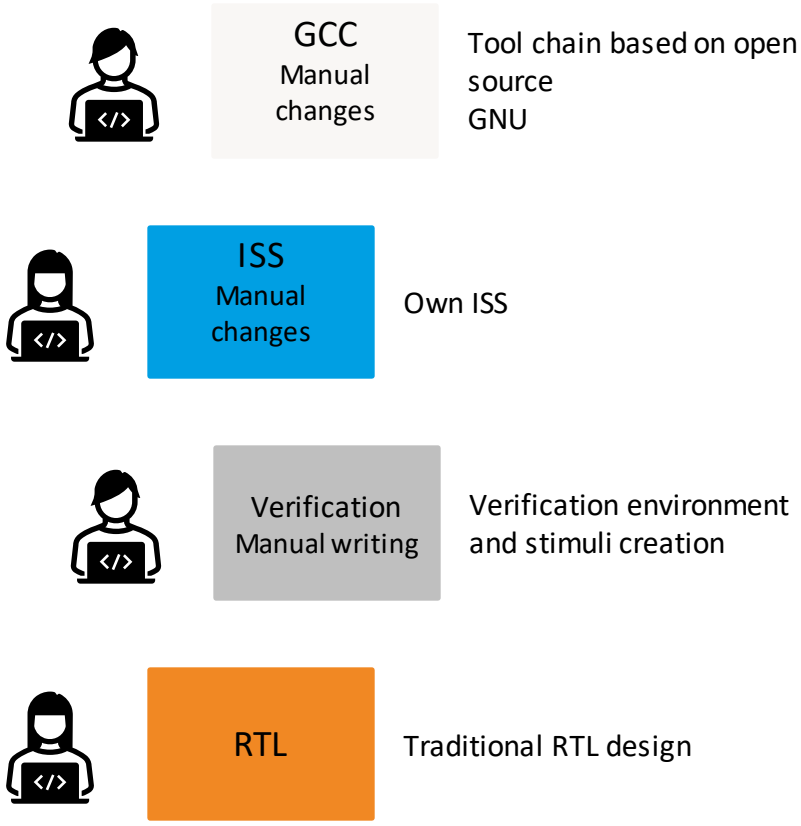
Revolutionizing processor design
by championing Custom Compute…

…optimizing the processor for the given software.

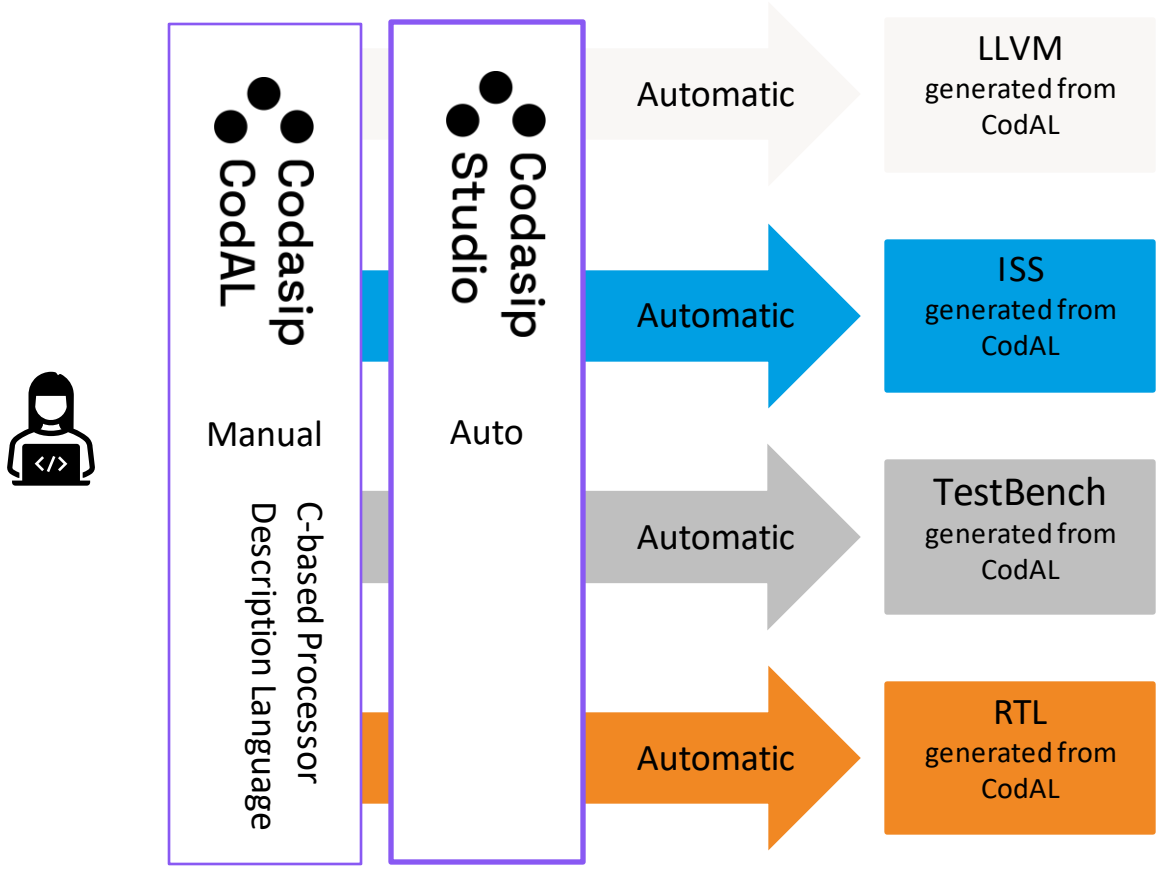
→ Codasip automates design (edA)

Improved efficiency, better results – Infinite variants

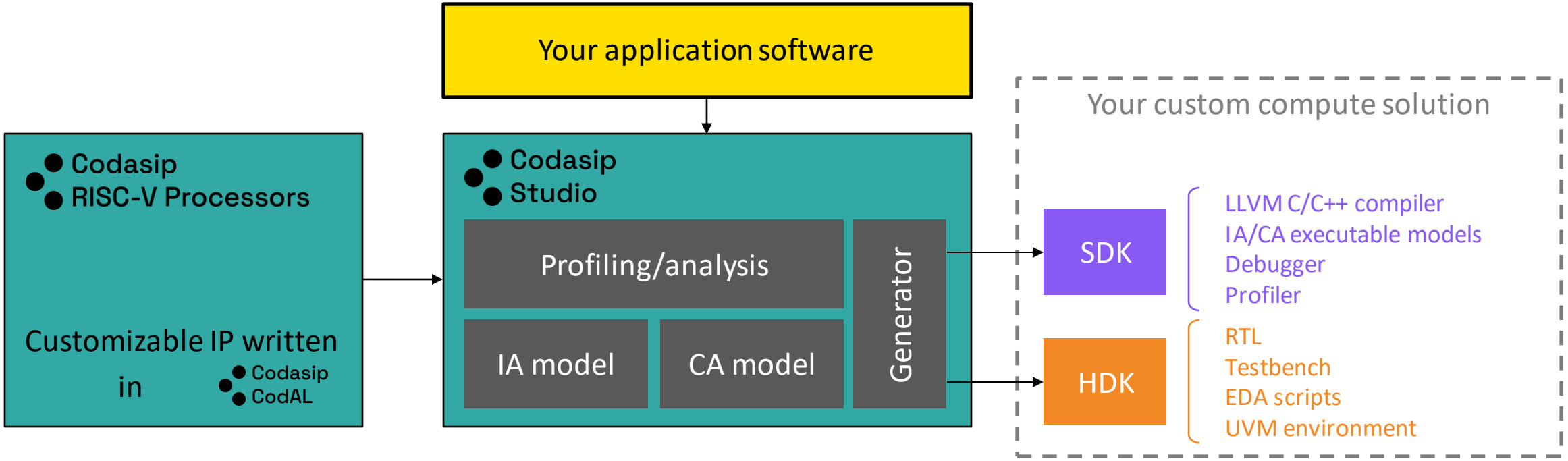
Old manual way – separated teams



Automated the Codasip way



→ How it works with Studio & our RISC-V cores



- Production-ready processors
  - Designed for customization
  - Fully RISC-V compliant
  - Best-in-class verification
- Differentiate with Codasip Studio
  - Profile / Configure / Modify
  - Using CodAL as input – high-level architecture description language

→ Codasip GPP Roadmap

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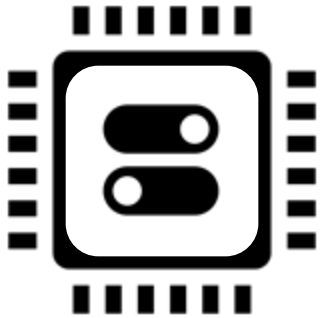
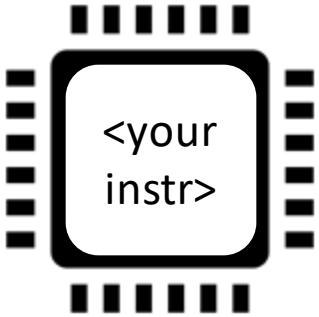
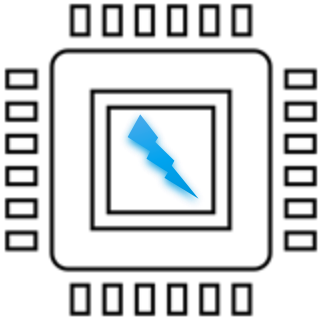
Codasip Studio



Custom
Configuration



Custom
Bounded



Custom
Design

→ Codasip GPP Roadmap

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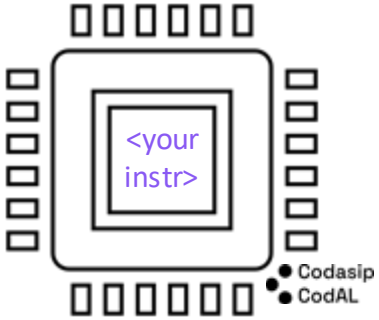
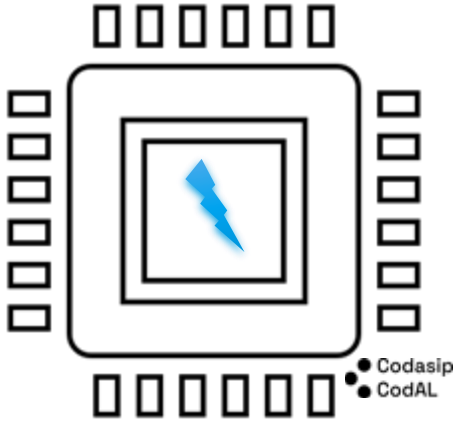
Performance

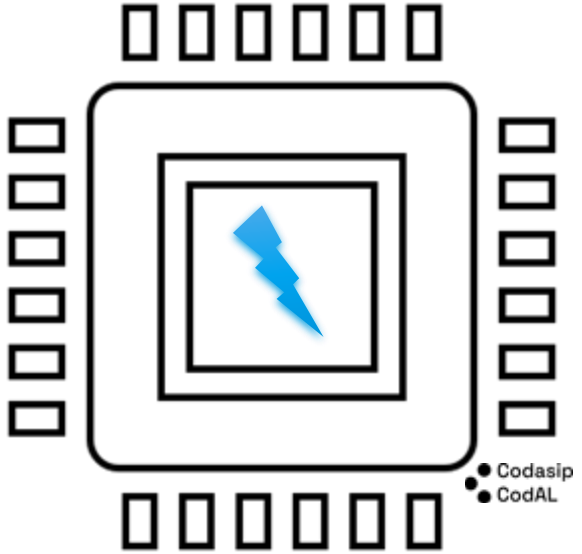
Super-scaler
Out-of-Order
Vector Compute



2 Issue



4 Issue



8 Issue

In-Order
Multi Issue

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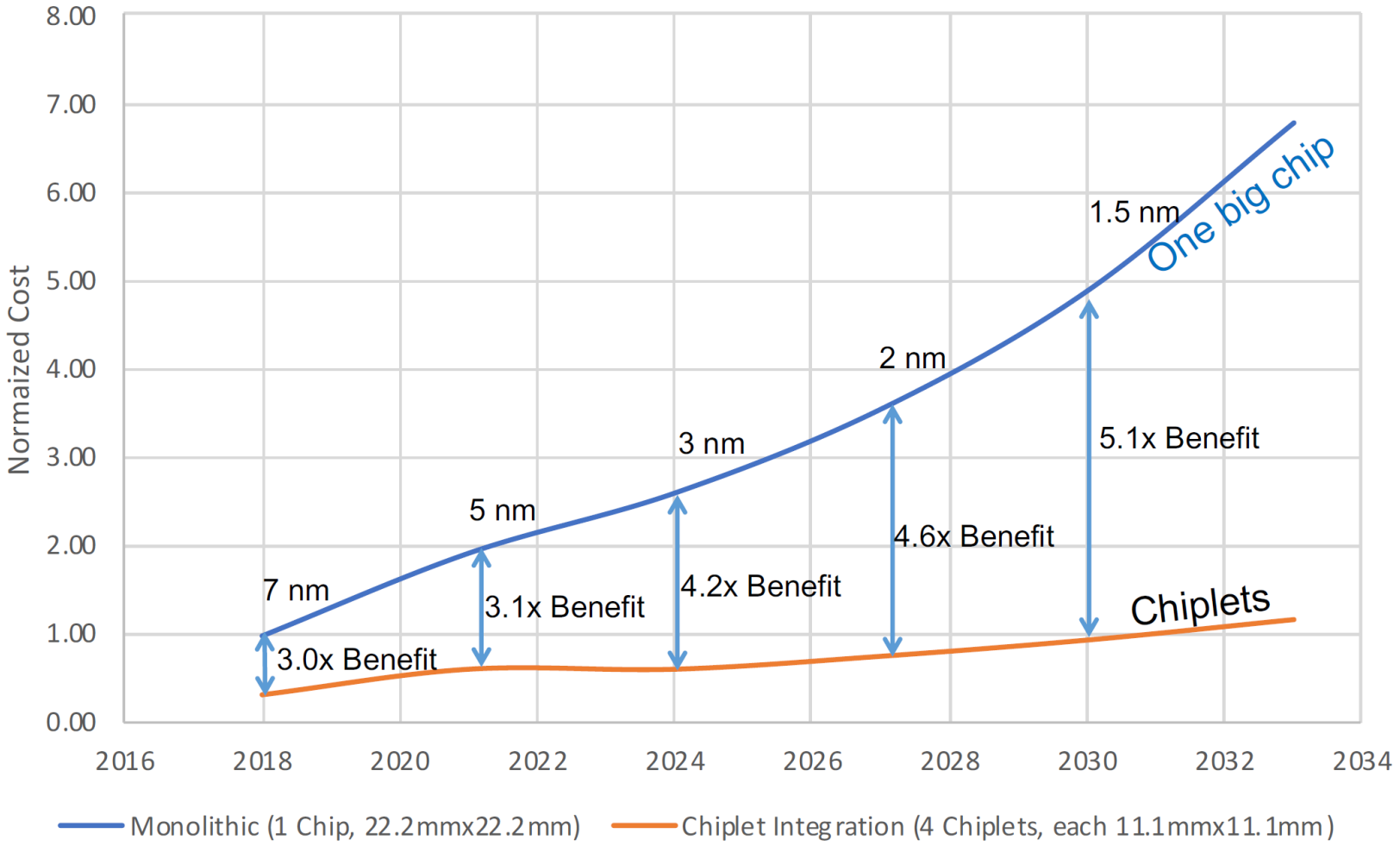
Common high-level
One source repository
Countless variants

Complexity (issue width)

→ Custom Chip Design via Chiplet

Example: Relative cost of ONE monolithic 500 mm^2 die vs implementing as FOUR 125mm^2 chiplets



Same design,
but on 4 chips vs 1 chip

Same total chip area

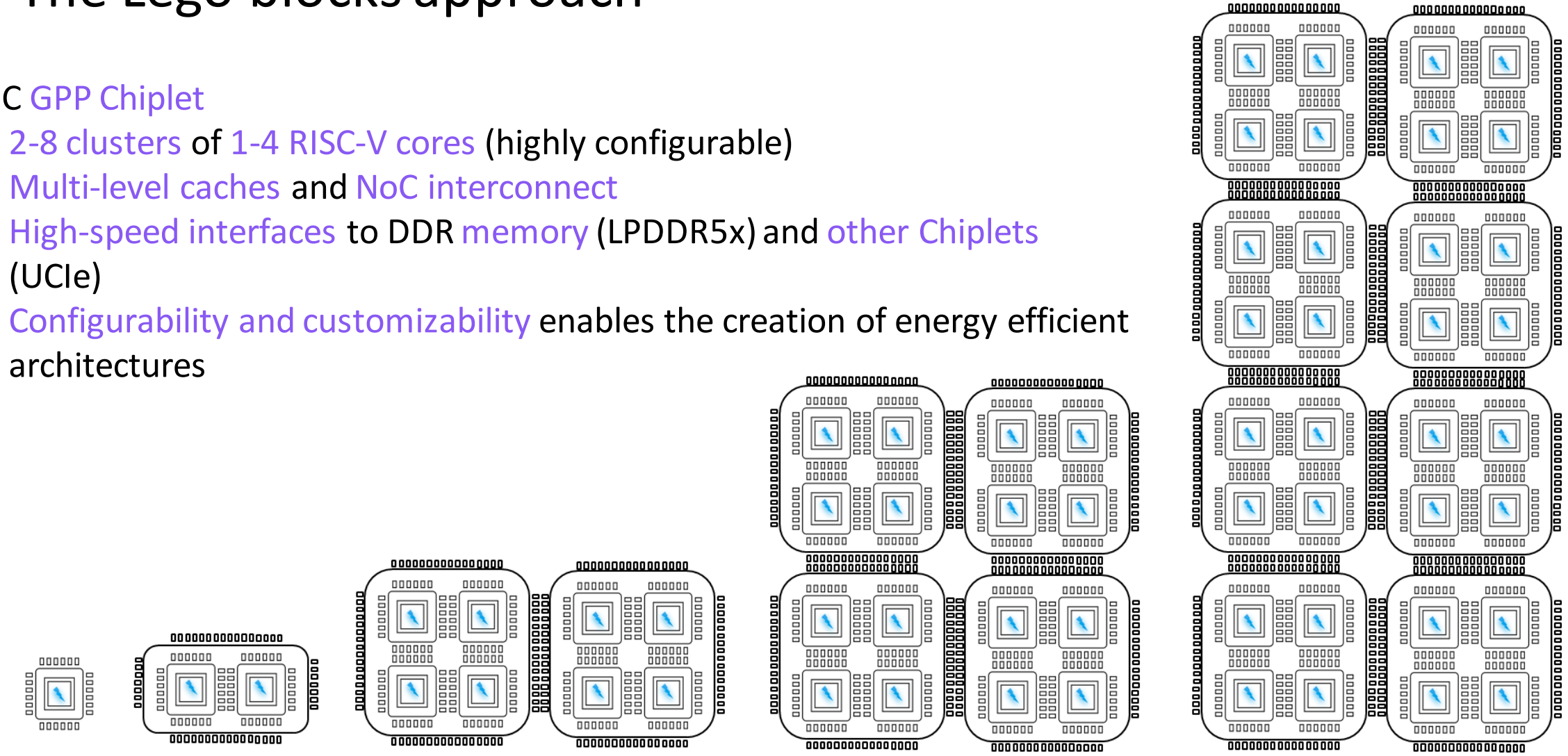
4 chips includes extra
testing and assembly cost

Chiplet gains could be more
when some pieces done
in older less expensive nodes

→ Enabling energy efficient chips: The Lego blocks approach

HPC GPP Chiplet

- 2-8 clusters of 1-4 RISC-V cores (highly configurable)
- Multi-level caches and NoC interconnect
- High-speed interfaces to DDR memory (LPDDR5x) and other Chiplets (UCIe)
- Configurability and customizability enables the creation of energy efficient architectures



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Thank you!